LogiCORE IP XPS LL TEMAC (v2.03a)

DS537June 23, 2010 Product Specification

Introduction

This document provides the design specification for the XPS_LL_TEMAC soft Ethernet core. This core provides a control interface to internal registers via a 32-bit Processor Local Bus (PLB) Version 4.6 as described in the *IBM CoreConnect 128-Bit Processor Local Bus, Architectural Specification Version 4.6*. This PLB slave interface supports single beat read and write data transfers (no burst transfers).

The transmit and receive data interface is via a Xilinx LocalLink Bus interface as described in this document.

TEMAC is an acronym for Tri-Mode Ethernet Media Access Controller and is a reference to the three speed (10, 100, and 1000 Mb/S) capable Ethernet MAC function available in this core.

This core is based on the Xilinx hard silicon Ethernet MAC in the Virtex-6, Virtex-5 FXt, LXt, and SXt and Virtex-4 FX devices and provides a soft Ethernet MAC option for those and other supported devices.

This core has been designed incorporating the applicable features described in IEEE Std. 802.3-2002.

Features

- Independent 2K, 4K, 8K, 16K, or 32K Byte TX and RX data FIFOs for queueing frames
- Filtering of "bad" receive frames
- Support for several PHY interfaces
- Media Independent Interface Management access to PHY registers
- Full-Duplex operation
  - Half-duplex is not supported
- Optional support for jumbo frames up to 9K Bytes
- Optional TX and RX TCP/UDP partial checksum off load in hardware
- Support for VLAN frames
- Optional TX and RX VLAN tagging, stripping, and translation

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Spartan®-3A/3A DSP, Spartan-3, Spartan-3E, Automotive Spartan 3/3E/3A/3A DSP, Spartan-6, Virtex®-4 /4Q/4QV, Virtex-5/5FX, Virtex-6/6CX	
Version of core	xps_ll_temac	v2.03a
Resources Used	See Table 138, Table 139, Table 140, Table 141, and Table 142.	
Special Features	None	
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	UCF	
Verification	VHDL Test bench	
Instantiation Template	VHDL Wrapper	
Reference Designs and application notes	None	
Additional Items	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE® 11.4 or later	
Verification	Mentor Graphics ModelSim PE/SE 6.4b or later	
Simulation	Mentor Graphics ModelSim PE/SE 6.4b or later	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

Features (contd)

- Support for Pause frames for flow control
- Optional extended filtering for multicast frames
- Optional TX and RX statistics gathering
- Auto PAD and FCS field insertion or pass through on transmit
- Auto PAD and FCS field stripping or pass through on receive
- One or two full duplex Ethernet bus interfaces with a shared control interface and independent data and interrupt interfaces
- Ethernet Audio Video Bridging (AVB) at 100/1000Mbs

Known Issues

Please reference the change log for known issues.

How To Use This Document

Some of the information in this document is identical or very similar for all modes of the xps_ll_temac. The first sections of this document will provide that information. In the cases where slight differences occur for a particular mode, footnotes will be used to call attention to the variance.

Other information in this document is specific to either the type of TEMAC or PHY interface selected. Following the sections containing the common information will be sections specific to Virtex-6 FPGA Hard TEMAC, Virtex-5 FPGA Hard TEMAC, Virtex-4 FPGA Hard TEMAC, and Soft TEMAC implementations.

Within these sections will be separate sections for each of the supported PHY interfaces.

Some users may wish to enjoy the entirety of this exciting document while others, more pressed for time, may wish to refer only to the common information and the sections for the specific TEMAC type and PHY interface they will be using.

Description

An XPS_LL_TEMAC provides additional functionality and ease of use to the Hard TEMAC silicon component that is built into some Virtex6, Virtex-5 and Virtex-4 FPGA devices while providing a soft Ethernet MAC option for all of the devices types that are supported. The main XPS_LL_TEMAC core uses several “helper” cores as needed for user selected functions.

The soft TEMAC is based on the Xilinx Coregen Tri Mode Ethernet MAC LogiCORE™. The Virtex-6 FPGA TEMAC is based on the Xilinx Coregen Virtex-6 Embedded Tri Mode Ethernet MAC LogiCORE. The Virtex-5 FPGA TEMAC is based on the Xilinx Coregen Virtex-5 FPGA Embedded Tri Mode Ethernet MAC LogiCORE. The Virtex-4 FPGA TEMAC is based on the Xilinx Coregen Virtex-4 FPGA Embedded Tri Mode Ethernet MAC LogiCORE. The statistics function is based on the Xilinx Coregen Ethernet Statistics LogiCORE. The Ethernet AVB Endpoint is based on the Xilinx Coregen Ethernet AVB Endpoint LogiCORE.

A high level block diagram of the XPS_LL_TEMAC IP core is shown in Figure 1. When the xps_ll_temac is used with either the Virtex-6, Virtex-5 or Virtex-4 FPGA hard TEMAC modes, the core is free and does not require a license.

When the xps_ll_temac is used with the soft TEMAC mode it will operate in an evaluation mode to allow users to determine if they would like to purchase a license for the full version of the core.

During evaluation modes, the core is fully functional but will only operate for several hour before requiring a reset to continue.

For more information on the Virtex-4, Virtex-5, and Virtex-6 FPGA Hard TEMAC silicon components, see the UG074 *Virtex-4 Embedded Tri-Mode Ethernet MAC User Guide v1.9*, UG194 *Virtex-5 Embedded Tri-Mode Ethernet MAC User Guide*, and UG368 *Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC User Guide*. For more information on the soft Tri Mode Ethernet MAC LogiCORE, see the UG138 *LogicCORE Tri-Mode Ethernet MAC User Guide*. For more information on the Ethernet statistics LogiCORE, see the UG170 *LogicCORE IP Ethernet Statistics User Guide*. For more information on the Ethernet AVB endpoint LogiCORE™, please refer to the *LogicCORE™ IP Ethernet AVB Endpoint User Guide* UG492.

The XPS_LL_TEMAC provides a standard PLB bus interface for a simple connection to PowerPC and MicroBlaze processor cores to allow access to the registers.

Xilinx LocalLink 32-bit buses are provided for moving transmit and receive Ethernet data to and from the XPS_LL_TEMAC. These buses are designed to provide direct connections to the built-in DMA function in some Virtex-5 devices or may be used with a soft DMA IP core or any other custom logic in any supported device. The LocalLink buses are designed to provide support for TCP/UDP partial checksum off load in hardware if that function is required. The LocalLink buses will be described later in this document.

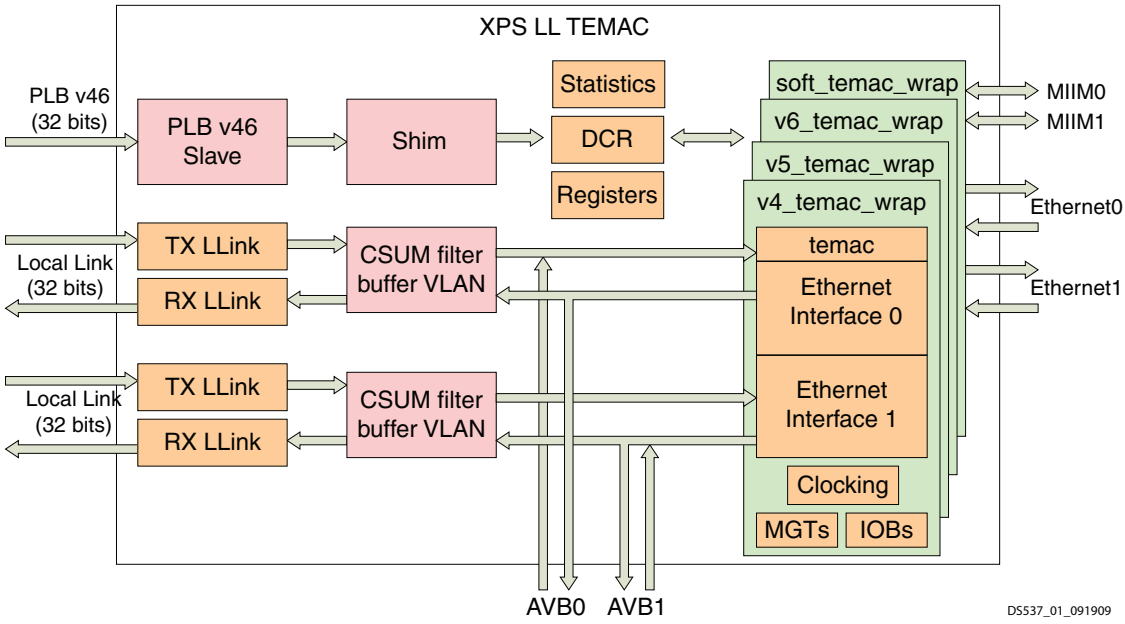

Figure 1: **XPS_LL_TEMAC Block Diagram**

The XPS_LL_TEMAC provides basic interrupt generation and control with interrupt control registers. The interrupt function will be described in more detail later in this document.

Support for many PHY interfaces is included and is selected with parameters at build time. The PHY interface support varies based on the TEMAC type selected. Please refer to Table 1.

The MII interface is supported for 10 and 100 Mbs and the 1000 Base-X interface is support for 1000 Mbs. The GMII/MII, RGMII v1.3, RGMII v2.0, and SGMII interfaces support all three speeds.

Table 1: **PHY Interface Support Based on TEMAC Mode Selected**

PHY Interface	Soft TEMAC	V4 Hard TEMAC	V5 Hard TEMAC	V6 Hard TEMAC
MII (10/100 Mbs)	Yes	Yes	Yes	Yes(1)
GMII/MII (tri-speed)	Yes	Yes	Yes	Yes(2)
RGMII V1.3 (tri-speed)	No	Yes	Yes	Yes
RGMII V2.0 (tri-speed)	No	No(3)	Yes	Yes
SGMII (tri-speed)	No	Yes	Yes	Yes
1000 Base-X (1000 Mbs)	No	Yes	Yes	Yes

1. Virtex®-6 devices support MII at 2.5 V only; Virtex-5, Virtex-4, Spartan®-6 and Spartan-3 devices support MII at 3.3 V or lower.
2. Virtex®-6 devices support GMII/MII at 2.5 V only; Virtex-5, Virtex-4, Spartan®-6 and Spartan-3 devices support GMII/MII at 3.3 V or lower.
3. Many PHY devices which support RGMII V2.0 will also work with RGMII V1.3 by adjusting some values in the PHY registers and by adjusting the DELAY primitives for the RGMII signals in the xps_ll_temac.

Table 2: **TEMAC Types Support Based on Device Selected**

C_FAMILY and C_SUBFAMILY	Soft TEMAC	V4 Hard TEMAC	V5 Hard TEMAC	V6 Hard TEMAC
SPARTAN3E	Yes	No	No	No
ASPARTAN3E	Yes	No	No	No
SPARTAN3A	Yes	No	No	No
ASPARTAN3A	Yes	No	No	No
SPARTAN3AN	Yes	No	No	No
SPARTAN3ADSP	Yes	No	No	No
ASPARTAN3ADSP	Yes	No	No	No
SPARTAN6	Yes	No	No	No
VIRTEX4 and LX	Yes	No	No	No
VIRTEX4 and SX	Yes	No	No	No
VIRTEX4 and FX	Yes	Yes	No	No
QVIRTEX4 and LX	Yes	No	No	No
QVIRTEX4 and SX	Yes	No	No	No
QVIRTEX4 and FX	Yes	Yes	No	No
QRVIRTEX4 and LX	Yes	No	No	No
QRVIRTEX4 and SX	Yes	No	No	No
QRVIRTEX4 and FX	Yes	Yes	No	No
VIRTEX5 and LX	Yes	No	No	No
VIRTEX5 and LXT	Yes	No	Yes	No
VIRTEX5 and SXT	Yes	No	Yes	No

Table 2: **TEMAC Types Support Based on Device Selected**

C_FAMILY and C_SUBFAMILY	Soft TEMAC	V4 Hard TEMAC	V5 Hard TEMAC	V6 Hard TEMAC
VIRTEX5 and FXT	Yes	No	Yes	No
VIRTEX6	Yes	No	No	Yes

Some of the functions optionally provided by the XPS_LL_TEMAC are not compatible with other optional functions. Figure 2 shows which optional functions are compatible with each other.

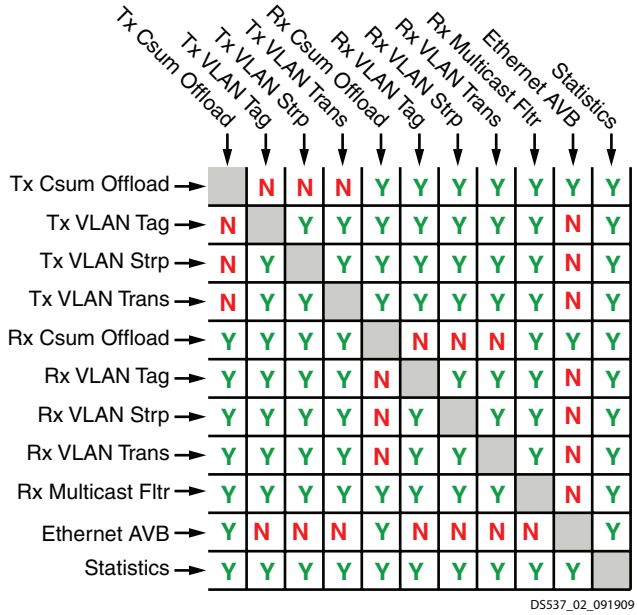

Figure 2: **Option Function Compatibility**

The XPS_LL_TEMAC provides one or two Ethernet interfaces. If two Ethernet interfaces are selected they are completely independent except that they must use the same type of PHY interface.

Access to external PHY registers is provided via a standard MII Management bus. A separate Management bus is provided for each of the Ethernet Interfaces. When using the SGMII or 1000 Base-X PHY interfaces, the XPS_LL_TEMAC provides some PHY functionality and as a result also includes PHY registers which are also accessible via the MII Management bus. These registers will be described later in this document.

This core optionally includes logic which helps calculate TCP/UDP checksums for transmit and verify TCP/UDP checksums for receive. Using this logic can significantly increase the maximum Ethernet bus data rate while reducing utilization of the processor for Ethernet tasks. Including the checksum off load function will increase the amount of FPGA resources used for this core. The checksum information is included with each Ethernet frame passing over the LocalLink bus interface. The checksum off load functionality can not be used at the same time as the extended VLAN functionality.

The XPS_LL_TEMAC provides FIFO buffering of transmit and receive Ethernet frames allowing more optimal transfer to and from the core with DMA. The number of frames that can be buffered in each direction is based on the size of each frame and the size of the FIFOs which are selected by parameters at build time. If the XPS_LL_TEMAC transmit FIFO becomes full it will throttle the transmit LocalLink interface until more room is available for Ethernet frames. If the receive FIFO becomes full, frames will

be dropped until more FIFO room is available. Receive frames that do not meet Ethernet format rules or do not satisfy receive address qualification will always be dropped.

Optional logic can be included to facilitate handling of VLAN type frames. Auto insertion, stripping, or translation of VLAN frames can be performed on transmit or receive with a number of options for choosing which frames will be altered.

Additional logic may be selected to provide additional filtering of receive frames with multicast destination addresses. The XPS_LL_TEMAC provides native support for up to 4 multicast addresses and the optional enhanced logic can support many more.

Logic may be selected to gather statistics on transmit and receive frames. This logic provides 64-bit counters for many statistics about the frames passing through the TEMAC core.

Support from Ethernet AVB may be included in the design. Ethernet AVB only supports Ethernet speeds of 100Mbs and 1000Mbs.

I/O Signals

The XPS_LL_TEMAC signals are listed and described in Table 3.

Table 3: **I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
TEMAC PLB Slave Signals				
SPLB_Clk	PLB	I		PLB Clock
SPLB_Rst(1)	PLB	I		PLB Reset
PLB_ABus(0:31)	PLB	I		PLB address bus
PLB_PAValid	PLB	I		PLB primary address valid indicator
PLB_masterID(0:C_SPLB_MID_WIDTH-1)	PLB	I		PLB requesting master identification
PLB_RNW	PLB	I		PLB read not write
PLB_BE(0:(C_SPLB_DWIDTH/8)-1)	PLB	I		PLB byte enables
PLB_size(0:3)	PLB	I		PLB transfer size
PLB_type(0:2)	PLB	I		PLB transfer type
PLB_wrDBus(0:C_SPLB_DWIDTH-1)	PLB	I		PLB write data bus
Sl_addrAck	PLB	O	0	Slave address acknowledge
Sl_SSize(1:0)	PLB	O	0	Slave data bus size
Sl_wait	PLB	O	0	Slave wait indicator
Sl_rearbitrate	PLB	O	0	Slave rearbitrate bus indicator
Sl_wrDack	PLB	O	0	Slave write data acknowledge
Sl_wrComp	PLB	O	0	Slave write transfer complete indicator

Table 3: **I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
Sl_rdBus(0:C_SPLB_DWIDTH-1)	PLB	O	0	Slave read bus
Sl_rdDAck	PLB	O	0	Slave read data acknowledge
Sl_rdComp	PLB	O	0	Slave read transfer complete indicator
Sl_MBusy(0:C_SPLB_NUM_MASTERS-1)	PLB	O	0	Slave busy indicator (1 bit for each PLB master)
Sl_MWrErr(0:C_SPLB_NUM_MASTERS-1)	PLB	O	0	Slave write error indicator (1 bit for each PLB master)
SlMRdErr(0:C_SPLB_NUM_MASTERS-1)	PLB	O	0	Slave read error indicator (1 bit for each PLB master)
Unused PLB Slave Signals				
PLB_UABus(0:31)	PLB	I		PLB upper address bus
PLB_SAValid	PLB	I		PLB secondary address valid indicator
PLB_rdPrim	PLB	I		PLB secondary to primary read request promotion
PLB_wrPrim	PLB	I		PLB secondary to primary write request promotion
PLB_abort	PLB	I		PLB bus request abort
PLB_buslock	PLB	I		PLB bus lock
PLB_MSize(0:1)	PLB	I		PLB master data bus size
PLB_TAttribute(0:15)	PLB	I		PLB transfer attribute bus
PLB_lockErr	PLB	I		PLB lock error
PLB_wrBurst	PLB	I		PLB write burst transfer
PLB_rdBurst	PLB	I		PLB read burst transfer
PLB_wrPendReq	PLB	I		PLB pending write request
PLB_rdPendReq	PLB	I		PLB pending read request
PLB_wrPendPri(0:1)	PLB	I		PLB pending write request priority
PLB_rdPendPri(0:1)	PLB	I		PLB pending read request priority
PLB_reqPri(0:1)	PLB	I		PLB current request priority
Sl_wrBTerm	PLB	O	0	Slave terminate write burst transfer
Sl_rdWdAddr(0:3)	PLB	O	0	Slave read word address
Sl_rdBTerm	PLB	O	0	Slave read burst terminate indicator
Sl_MIRQ(0:C_PLB_NUM_MASTERS-1)	PLB	O	0	Slave interrupt indication (1 bit for each PLB master)
LocalLink Signals				
LlinkTemac0_CLK (2)	LLink 0	I		LocalLink to TEMAC LocalLink clock

Table 3: **I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
LLinkTemac0_RST	LLink 0	I		LocalLink to TEMAC LocalLink reset
LlinkTemac0_SOP_n	LLink 0	I		LocalLink to TEMAC LocalLink Start of Payload indicator
LlinkTemac0_EOP_n	LLink 0	I		LocalLink to TEMAC LocalLink End of Payload indicator
LlinkTemac0_SOF_n	LLink 0	I		LocalLink to TEMAC LocalLink Start of Frame indicator
LlinkTemac0_EOF_n	LLink 0	I		LocalLink to TEMAC LocalLink End of Frame indicator
LlinkTemac0_REM(0:3)	LLink 0	I		LocalLink to TEMAC LocalLink last word byte valid indicator
LlinkTemac0_Data(0:31)	LLink 0	I		LocalLink to TEMAC LocalLink transmit data
LlinkTemac0_SRC_RDY_n	LLink 0	I		LocalLink to TEMAC LocalLink ready to send data indicator
Temac0Llink_DST_RDY_n	LLink 0	O	0	TEMAC to LocalLink LocalLink ready to receive data indicator
Temac0Llink_SOP_n	LLink 0	O	1	TEMAC to LocalLink LocalLink Start of Payload indicator
Temac0Llink_EOP_n	LLink 0	O	1	TEMAC to LocalLink LocalLink End of Payload indicator
Temac0Llink_SOF_n	LLink 0	O	1	TEMAC to LocalLink LocalLink Start of Frame indicator
Temac0Llink_EOF_n	LLink 0	O	1	TEMAC to LocalLink LocalLink End of Frame indicator
Temac0Llink_REM(0:3)	LLink 0	O	0	TEMAC to LocalLink LocalLink last word byte valid indicator
Temac0Llink_Data(0:31)	LLink 0	O	0	TEMAC to LocalLink LocalLink receive data
Temac0Llink_SRC_RDY_n	LLink 0	O	0	TEMAC to LocalLink LocalLink ready to send data indicator
LlinkTemac0_DST_RDY_n	LLink 0	I		LocalLink to TEMAC LocalLink ready to receive data indicator
LlinkTemac1_CLK(2)	LLink 1	I		LocalLink to TEMAC LocalLink clock
LLinkTemac1_RST	LLink 1	I		LocalLink to TEMAC LocalLink reset
LlinkTemac1_SOP_n	LLink 1	I		LocalLink to TEMAC LocalLink Start of Payload indicator
LlinkTemac1_EOP_n	LLink 1	I		LocalLink to TEMAC LocalLink End of Payload indicator
LlinkTemac1_SOF_n	LLink 1	I		LocalLink to TEMAC LocalLink Start of Frame indicator

Table 3: **I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
LlinkTemac1_EOF_n	LLink 1	I		LocalLink to TEMAC LocalLink End of Frame indicator
LlinkTemac1_REM(0:3)	LLink 1	I		LocalLink to TEMAC LocalLink last word byte valid indicator
LlinkTemac1_Data(0:31)	LLink 1	I		LocalLink to TEMAC LocalLink transmit data
LlinkTemac1_SRC_RDY_n	LLink 1	I		LocalLink to TEMAC LocalLink ready to send data indicator
Temac1Llink_DST_RDY_n	LLink 1	O	0	TEMAC to LocalLink LocalLink ready to receive data indicator
Temac1Llink_SOP_n	LLink 1	O	1	TEMAC to LocalLink LocalLink Start of Payload indicator
Temac1Llink_EOP_n	LLink 1	O	1	TEMAC to LocalLink LocalLink End of Payload indicator
Temac1Llink_SOF_n	LLink 1	O	1	TEMAC to LocalLink LocalLink Start of Frame indicator
Temac1Llink_EOF_n	LLink 1	O	1	TEMAC to LocalLink LocalLink End of Frame indicator
Temac1Llink_REM(0:3)	LLink 1	O	0	TEMAC to LocalLink LocalLink last word byte valid indicator
Temac1Llink_Data(0:31)	LLink 1	O	0	TEMAC to LocalLink LocalLink receive data
Temac1Llink_SRC_RDY_n	LLink 1	O	0	TEMAC to LocalLink LocalLink ready to send data indicator
LlinkTemac1_DST_RDY_n	LLink 1	I		LocalLink to TEMAC LocalLink ready to receive data indicator
Ethernet AVB Signals				
Temac0AvbTxClk	AVB 0	O		TEMAC to AVB Transmit Client Clock
Temac0AvbTxClkEn	AVB 0	O		TEMAC to AVB Transmit Client Clock Enable
Temac0AvbRxClk	AVB 0	O		TEMAC to AVB Receive Client Clock
Temac0AvbRxClkEn	AVB 0	O		TEMAC to AVB Receive Client Clock Enable
Avb2Mac0TxData	AVB 0	I	0	AVB to TEMAC Transmit Data
Avb2Mac0TxDataValid	AVB 0	I	0	AVB to TEMAC Transmit Data Valid indicator
Avb2Mac0TxUnderrun	AVB 0	I	0	AVB to TEMAC Transmit Underrun indicator
Mac02AvbTxAck	AVB 0	O	0	TEMAC to AVB Transmit Acknowledge indicator
Mac02AvbRxData	AVB 0	O	0	TEMAC to AVB Receive Data

Table 3: **I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
Mac02AvbRxDataValid	AVB 0	O	0	TEMAC to AVB Receive Data Valid indicator
Mac02AvbRxFrameGood	AVB 0	O	0	TEMAC to AVB Receive Frame Good indicator
Mac02AvbRxFrameBad	AVB 0	O	0	TEMAC to AVB Receive Frame Bad indicator
Temac02AvbTxData	AVB 0	O	0	TEMAC to AVB Transmit Data
Temac02AvbTxDataValid	AVB 0	O	0	TEMAC to AVB Transmit Data Valid indicator
Temac02AvbTxUnderrun	AVB 0	O	0	TEMAC to AVB Transmit Underrun indicator
Avb2Temac0TxAck	AVB 0	I	0	AVB to TEMAC Transmit Acknowledge indicator
Avb2Temac0RxData	AVB 0	I	0	AVB to TEMAC Receive Data
Avb2Temac0RxDataValid	AVB 0	I	0	AVB to TEMAC Receive Data Valid indicator
Avb2Temac0RxFrameGood	AVB 0	I	0	AVB to TEMAC Receive Frame Good indicator
Avb2Temac0RxFrameBad	AVB 0	I	0	AVB to TEMAC Receive Data Frame Bad indicator
Temac1AvbTxClk	AVB 1	O		TEMAC to AVB Transmit Client Clock
Temac1AvbTxClkEn	AVB 1	O		TEMAC to AVB Transmit Client Clock Enable
Temac1AvbRxClk	AVB 1	O		TEMAC to AVB Receive Client Clock
Temac1AvbRxClkEn	AVB 1	O		TEMAC to AVB Receive Client Clock Enable
Avb2Mac1TxData	AVB 1	I	0	AVB to TEMAC Transmit Data
Avb2Mac1TxDataValid	AVB 1	I	0	AVB to TEMAC Transmit Data Valid indicator
Avb2Mac1TxUnderrun	AVB 1	I	0	AVB to TEMAC Transmit Underrun indicator
Mac12AvbTxAck	AVB 1	O	0	TEMAC to AVB Transmit Acknowledge indicator
Mac12AvbRxData	AVB 1	O	0	TEMAC to AVB Receive Data
Mac12AvbRxDataValid	AVB 1	O	0	TEMAC to AVB Receive Data Valid indicator
Mac12AvbRxFrameGood	AVB 1	O	0	TEMAC to AVB Receive Frame Good indicator
Mac12AvbRxFrameBad	AVB 1	O	0	TEMAC to AVB Receive Frame Bad indicator
Temac12AvbTxData	AVB 1	O	0	TEMAC to AVB Transmit Data

Table 3: **I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
Temac12AvbTxDataValid	AVB 1	O	0	TEMAC to AVB Transmit Data Valid indicator
Temac12AvbTxUnderrun	AVB 1	O	0	TEMAC to AVB Transmit Underrun indicator
Avb2Temac1TxAck	AVB 1	I	0	AVB to TEMAC Transmit Acknowledge indicator
Avb2Temac1RxData	AVB 1	I	0	AVB to TEMAC Receive Data
Avb2Temac1RxDataValid	AVB 1	I	0	AVB to TEMAC Receive Data Valid indicator
Avb2Temac1RxFrameGood	AVB 1	I	0	AVB to TEMAC Receive Frame Good indicator
Avb2Temac1RxFrameBad	AVB 1	I	0	AVB to TEMAC Receive Data Frame Bad indicator
System Signals				
Core_Clk	System	I		1/2 frequency clock input derived from SPLB_Clk used internally for PLB accesses when C_BUS2CORE_CLK_RATIO = 2
TemacIntc0_Irpt	System	O	0	Interrupt indicator for TEMAC 0
TemacIntc1_Irpt	System	O	0	Interrupt indicator for TEMAC 1
Ethernet System Signals				
TemacPhy_RST_n	Ethernet	O	0	TEMAC to PHY reset signal connected internally to the inverse of the SPLB_Rst input. The PHY is reset whenever the SPLB is reset
REFCLK(3)	Ethernet	I		200 MHz input clock on global clock routing used for signal delay primitives for all GMII and RGMII PHY modes, and when Ethernet Statistics are enabled for all device families other than Spartan-6
DCLK	Ethernet	I		25 MHz to 50 MHz input clock on global clock routing used for dynamic reconfiguration for Virtex-4 hard TEMAC SGMII and 1000 Base-X PHY modes
GTX_CLK_0(4)	Ethernet	I		125 MHz input clock on global clock routing used to derive the other transmit clocks for all GMII and RGMII PHY modes. For soft TEMAC MII PHY systems, this clock must be driven by some clock (does not need to be 125 MHz). The PLB clock may be used in these cases. Also used when Ethernet Statistics are enabled with the Spartan-6 device family

Table 3: **I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
MGTCLK_P	Ethernet	I		Positive polarity of differential clock used to drive RocketIO™ MGTs. Must be connected to an external, high-quality differential reference clock of frequency of 125 MHz for Virtex-5 and 250 MHz for Virtex-4.(5)
MGTCLK_N	Ethernet	I		Negative polarity of differential clock used to drive RocketIO MGTs.Must be connected to an external, high-quality differential reference clock of frequency of 125 MHz for Virtex-5 and 250 MHz for Virtex-4.(5).
Ethernet Channel 0 MII Signals				
MII_TXD_0(3:0)	Ethernet bus 0 MII	O	0	TEMAC to PHY transmit data
MII_TX_EN_0	Ethernet bus 0 MII	O	0	TEMAC to PHY transmit enable
MII_TX_ER_0	Ethernet bus 0 MII	O	0	TEMAC to PHY transmit Error enable
MII_RXD_0(3:0)	Ethernet bus 0 MII	I		PHY to TEMAC receive data
MII_RX_DV_0	Ethernet bus 0 MII	I		PHY to TEMAC receive data valid indicator
MII_RX_ER_0	Ethernet bus 0 MII	I		PHY to TEMAC receive error indicator
MII_RX_CLK_0	Ethernet bus 0 MII	I		PHY to TEMAC receive clock
MII_TX_CLK_0	Ethernet bus 0 MII	I		PHY to TEMAC transmit clock (also used for GMII/MII mode)
Ethernet Channel 1 MII Signals				
MII_TXD_1(3:0)	Ethernet bus 1 MII	O	0	TEMAC to PHY transmit data
MII_TX_EN_1	Ethernet bus 1MII	O	0	TEMAC to PHY transmit enable
MII_TX_ER_1	Ethernet bus 1 MII	O	0	TEMAC to PHY transmit Error enable
MII_RXD_1(3:0)	Ethernet bus 1 MII	I		PHY to TEMAC receive data
MII_RX_DV_1	Ethernet bus 1 MII	I		PHY to TEMAC receive data valid indicator
MII_RX_ER_1	Ethernet bus 1 MII	I		PHY to TEMAC receive error indicator
MII_RX_CLK_1	Ethernet bus 1 MII	I		PHY to TEMAC receive clock

Table 3: **I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
MII_TX_CLK_1	Ethernet bus 1 MII	I		PHY to TEMAC transmit clock (also used for GMII/MII mode)
Ethernet Channel 0 GMII Signals				
GMII_TXD_0(7:0)	Ethernet bus 0 GMII	O	0	TEMAC to PHY transmit data
GMII_TX_EN_0	Ethernet bus 0 GMII	O	0	TEMAC to PHY transmit enable
GMII_TX_ER_0	Ethernet bus 0 GMII	O	0	TEMAC to PHY transmit Error enable
GMII_TX_CLK_0	Ethernet bus 0 GMII	O	0	TEMAC to PHY transmit clock
GMII_RXD_0(7:0)	Ethernet bus 0 GMII	I		PHY to TEMAC receive data
GMII_RX_DV_0	Ethernet bus 0 GMII	I		PHY to TEMAC receive data valid indicator
GMII_RX_ER_0	Ethernet bus 0 GMII	I		PHY to TEMAC receive error indicator
GMII_RX_CLK_0	Ethernet bus 0 GMII	I		PHY to TEMAC receive clock
Ethernet Channel 1 GMII Signals				
GMII_TXD_1(7:0)	Ethernet bus 1 GMII	O	0	TEMAC to PHY transmit data
GMII_TX_EN_1	Ethernet bus 1 GMII	O	0	TEMAC to PHY transmit enable
GMII_TX_ER_1	Ethernet bus 1 GMII	O	0	TEMAC to PHY transmit Error enable
GMII_TX_CLK_1	Ethernet bus 1 GMII	O	0	TEMAC to PHY transmit clock
GMII_RXD_1(7:0)	Ethernet bus 1 GMII	I		PHY to TEMAC receive data
GMII_RX_DV_1	Ethernet bus 1 GMII	I		PHY to TEMAC receive data valid indicator
GMII_RX_ER_1	Ethernet bus 1 GMII	I		PHY to TEMAC receive error indicator
GMII_RX_CLK_1	Ethernet bus 1 GMII	I		PHY to TEMAC receive clock
Ethernet Channel 0 SGMII and 1000Base-X Signals				
TXP_0	Ethernet bus 0 SGMII and 1000Base-X	O	0	TEMAC to PHY transmit data positive

Table 3: **I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
TXN_0	Ethernet bus 0 SGMII and 1000Base-X	O	0	TEMAC to PHY transmit data negative
RXP_0	Ethernet bus 0 SGMII and 1000Base-X	I		PHY to TEMAC receive data positive
RXN_0	Ethernet bus 0 SGMII and 1000Base-X	I		PHY to TEMAC receive data negative
Ethernet Channel 1 SGMII and 1000Base-X Signals				
TXP_1	Ethernet bus 1 SGMII and 1000Base-X	O	0	TEMAC to PHY transmit data positive
TXN_1	Ethernet bus 1 SGMII and 1000Base-X	O	0	TEMAC to PHY transmit data negative
RXP_1	Ethernet bus 1 SGMII and 1000Base-X	I		PHY to TEMAC receive data positive
RXN_1	Ethernet bus 1 SGMII and 1000Base-X	I		PHY to TEMAC receive data negative
Ethernet Channel 0 RGMII Signals				
RGMII_TXD_0(3:0)	Ethernet bus 0 RGMII	O	0	TEMAC to PHY transmit data
RGMII_TX_CTL_0	Ethernet bus 0 RGMII	O	0	TEMAC to PHY transmit control
RGMII_TXC_0	Ethernet bus 0 RGMII	O	0	TEMAC to PHY transmit clock
RGMII_RXD_0(3:0)	Ethernet bus 0 RGMII	I		PHY to TEMAC receive data

Table 3: **I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
RGMII_RX_CTL_0	Ethernet bus 0 RGMII	I		PHY to TEMAC receive control
RGMII_RXC_0	Ethernet bus 0 RGMII	I		PHY to TEMAC receive clock
Ethernet Channel 1 RGMII Signals				
RGMII_TXD_1(3:0)	Ethernet bus 1 RGMII	O	0	TEMAC to PHY transmit data
RGMII_TX_CTL_1	Ethernet bus 1 RGMII	O	0	TEMAC to PHY transmit control
RGMII_TXC_1	Ethernet bus 1 RGMII	O	0	TEMAC to PHY transmit clock
RGMII_RXD_1(3:0)	Ethernet bus 1 RGMII	I		PHY to TEMAC receive data
RGMII_RX_CTL_1	Ethernet bus 1 RGMII	I		PHY to TEMAC receive control
RGMII_RXC_1	Ethernet bus 1 RGMII	I		PHY to TEMAC receive clock
Ethernet Channel 0 MII Management Interface (MIIM) Signals				
MDC_0	Ethernet bus 0 MIIM	O	0	TEMAC to PHY MII management bus clock
MDIO_0	Ethernet bus 0 MIIM	I/O	0	TEMAC to/from PHY MII management data
Ethernet Channel 1 MII Management Interface (MIIM) Signals				
MDC_1	Ethernet bus 1 MIIM	O	0	TEMAC to PHY MII management bus clock
MDIO_1	Ethernet bus 1 MIIM	I/O	0	TEMAC to/from PHY MII management data
Host Read External Data Interface Signals(6)				
HostMiimRdy	Host Read	I		External Data to TEMAC read ready
HostRdData(31:0)	Host Read	I		External Data to TEMAC read data
HostMiimSel	Host Read	O	0	TEMAC to External Data Enable
HostReq	Host Read	O	0	TEMAC to External Data Read Request
HostAddr(9:0)	Host Read	O	0	TEMAC to External Data Read Address

Table 3: **I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
HostEmac1Sel	Host Read	O	0	TEMAC to External Data TEMAC 0 vs. TEMAC1 select
Ethernet Statistics Interface Signals				
TxClientClk_0	Statistics 0	O	0	TEMAC to Statistics TX Clock
ClientTxStat_0	Statistics 0	O	0	TEMAC to Statistics TX Data
ClientTxStatsVld_0	Statistics 0	O	0	TEMAC to Statistics TX Valid Indicator
ClientTxStatsByteVld_0	Statistics 0	O	0	TEMAC to Statistics TX Byte Valid Indicator
RxClientClk_0	Statistics 0	O	0	TEMAC to Statistics RX Clock
ClientRxStats_0(6:0)	Statistics 0	O	0	TEMAC to Statistics RX Data
ClientRxStatsVld_0	Statistics 0	O	0	TEMAC to Statistics RX Valid Indicator
ClientRxStatsByteVld_0	Statistics 0	O	0	TEMAC to Statistics RX Byte Valid Indicator
TxClientClk_1	Statistics 1	O	0	TEMAC to Statistics TX Clock
ClientTxStat_1	Statistics 1	O	0	TEMAC to Statistics TX Data
ClientTxStatsVld_1	Statistics 1	O	0	TEMAC to Statistics TX Valid Indicator
ClientTxStatsByteVld_1	Statistics 1	O	0	TEMAC to Statistics TX Byte Valid Indicator
RxClientClk_1	Statistics 1	O	0	TEMAC to Statistics RX Clock
ClientRxStats_1(6:0)	Statistics 1	O	0	TEMAC to Statistics RX Data
ClientRxStatsVld_1	Statistics 1	O	0	TEMAC to Statistics RX Valid Indicator
ClientRxStatsByteVld_1	Statistics 1	O	0	TEMAC to Statistics RX Byte Valid Indicator

1. This core is designed with only synchronous resets. As a consequence of this design methodology, slower clock domains will come out of reset before fast clock domains. For most systems this is not an issue, but for 10 Mbs operation, the slower tx client Ethernet core clock can be as low as 1.25 MHz. With such a slow clock and PLB running at 125 MHz, the circuit on the 1.25 MHz clock will come out of reset up to 800 ns (or 100 PLB clock periods) after the PLB clock domain comes out of reset. To insure proper core behavior, the TEMAC core should not be accessed for at least 800 ns after PLB reset.
2. The LocalLink clock must be equal to or greater than half the frequency of the Ethernet data on the PHY interface. When using a 1000 Mbs Ethernet bus speed, the PHY data clock is 125 MHz so the LocalLink clock must be 62.5 MHz or greater (faster). When using a 100 Mbs Ethernet bus speed, the PHY data clock is 25 MHz so the LocalLink clock must be 12.5 MHz or greater. When using a 10 Mbs Ethernet bus speed, the PHY data clock is 2.5 MHz so the LocalLink clock must be 1.25 MHz or greater.
3. When ethernet statistics are enabled with the Virtex-6, Virtex-5, Virtex-4, and Spartan-3 device families, the ethernet statistics core's reference clock is connected to REFCLK.
4. When ethernet statistics are enabled with the Spartan-6 device family, the ethernet statistics core's reference clock is connected to GTX_CLK_0.
5. Please refer to "1000BASE-X Auto-Negotiation" on page 134 for information on example system.ucf constraints that may be used to allow 125 MHz clocks in Virtex-4 and their limitations.
6. The Host Interface Signals are not used at this time and should always remain unconnected.

Design Parameters

To allow the user to generate an XPS_LL_TEMAC that is uniquely tailored the user's system, certain features can be parameterized in the XPS_LL_TEMAC design as shown in Table 4.

Table 4: **XPS_LL_TEMAC Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
User Specified PLB Bus Implementation Parameters				
PLB Base Address (1)	C_BASEADDR	Valid PLB Address	0xFFFFFFFF (2)	std_logic_vector
PLB High Address(3)	C_HIGHADDR	Valid PLB Address	0x00000000(2)	std_logic_vector
System Specified PLB Bus Implementation Parameters				
PLB Data Bus Width(4)	C_SPLB_DWIDTH	32	32	integer
PLB Address Bus Width(4)	C_SPLB_AWIDTH	32	32	integer
Number of Masters(4)	C_SPLB_NUM_MASTERS	1-16	8	integer
Width of Master ID Bus(4)	C_SPLB_MID_WIDTH	roundup($\log_2$(C_SPLB_NUM_MASTERS))	3	integer
Data width supported by this core	C_SPLB_NATIVE_DWIDTH	32	32	integer
Enable/Disable PLB Point to Point connection mode	C_SPLB_P2P	0	0	integer
Enable/Disable reduced internal PLB clock usage	C_BUS2CORE_CLK_RATIO	1 = internal clock equal to PLB clock 2 = internal clock is 1/2 of PLB clock (uses Core_Clk)	2	integer
Subfamily of FPGA device selected when applicable(4)	C_SUBFAMILY	Valid device subfamilies	"FX"	string
User Specified TEMAC Implementation Parameters				
Reserved	C_RESERVED	0	0	integer
Number of IDELAYCTRLs required(5)	C_NUM_IDELAYCTRL	0-16	0	Integer
Location of IDELAYCTRLs(5)	C_IDELAYCTRL_LOC	Valid IDELAYCTRL Locations	""	String

Table 4: **XPS_LL_TEMAC Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
FPGA Device Family Selected(4)	C_FAMILY	VIRTEX6, VIRTEX5, VIRTEX4, QVIRTEX4, QRVIRTEX4, SPARTAN3E, ASPARTAN3E, SPARTAN3A, ASPARTAN3A, SPARTAN3AN, SPARTAN3ADSP, ASPARTAN3ADSP, SPARTAN6	"VIRTEX 5"	string
Type of TEMAC selected	C_TEMAC_TYPE	0 = Virtex 5 Hard 1 = Virtex 4 Hard 2 = Soft 3 = Virtex 6 Hard	0	integer
INCLUDE I/O and BUFGs as needed for the PHY interface selected	C_INCLUDE_IO	1 = I/O included 0 = I/O not included	1	integer
PHY Interface Type	C_PHY_TYPE(6)	0 = MII 1 = GMII/MII 2 = RGMII V1.3 3 = RGMII v2.0 4 = SGMII 5 = 1000Base-X	1	integer
Enable use of TEMAC 1	C_TEMAC1_ENABLED	1 = TEMAC 1 used 0 = TEMAC 1 unused	0	integer
PHY Address for TEMAC 0	C_TEMAC0_PHYADDR(7)	00001 - 11111	00001	std_logic_vector
PHY Address for TEMAC 1	C_TEMAC1_PHYADDR(7)	00001 - 11111	00010	std_logic_vector
Transmit FIFO depth in Bytes for TEMAC 0	C_TEMAC0_TXFIFO(8)	2048, 4096, 8192, 16384, 32768	4096	integer
Receive FIFO depth in Bytes for TEMAC 0	C_TEMAC0_RXFIFO(8)	2048, 4096, 8192, 16384, 32768	4096	integer
Transmit FIFO depth in Bytes for TEMAC 1	C_TEMAC1_TXFIFO(8)	2048, 4096, 8192, 16384, 32768	4096	integer
Receive FIFO depth in Bytes for TEMAC 1	C_TEMAC1_RXFIFO(8)	2048, 4096, 8192, 16384, 32768	4096	integer
Transmit TCP/UDP Checksum off load for TEMAC 0	C_TEMAC0_TXCSUM	1 = Tx CSUM used 0 = Tx CSUM unused	0	integer
Receive TCP/UDP Checksum off load for TEMAC 0	C_TEMAC0_RXCSUM	1 = Rx CSUM used 0 = Rx CSUM unused	0	integer

Table 4: **XPS_LL_TEMAC Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
Transmit TCP/UDP Checksum off load for TEMAC 1	C_TEMAC1_TXCSUM	1 = Tx CSUM used 0 = Tx CSUM unused	0	integer
Receive TCP/UDP Checksum off load for TEMAC 1	C_TEMAC1_RXCSUM	1 = Rx CSUM used 0 = Rx CSUM unused	0	integer
Transmit VLAN tagging for TEMAC 0	C_TEMAC0_TXVLAN_TAG	1 = Tx VLAN tagging used 0 = Tx VLAN tagging unused	0	integer
Receive VLAN tagging for TEMAC 0	C_TEMAC0_RXVLAN_TAG	1 = Rx VLAN tagging used 0 = Rx VLAN tagging unused	0	integer
Transmit VLAN tagging for TEMAC 1	C_TEMAC1_TXVLAN_TAG	1 = Tx VLAN tagging used 0 = Tx VLAN tagging unused	0	integer
Receive VLAN tagging for TEMAC 1	C_TEMAC1_RXVLAN_TAG	1 = Rx VLAN tagging used 0 = Rx VLAN tagging unused	0	integer
Transmit VLAN translation for TEMAC 0	C_TEMAC0_TXVLAN_TRAN	1 = Tx VLAN translation used 0 = Tx VLAN translation unused	0	integer
Receive VLAN translation for TEMAC 0	C_TEMAC0_RXVLAN_TRAN	1 = Rx VLAN translation used 0 = Rx VLAN translation unused	0	integer
Transmit VLAN translation for TEMAC 1	C_TEMAC1_TXVLAN_TRAN	1 = Tx VLAN translation used 0 = Tx VLAN translation unused	0	integer
Receive VLAN translation for TEMAC 1	C_TEMAC1_RXVLAN_TRAN	1 = Rx VLAN translation used 0 = Rx VLAN translation unused	0	integer
Transmit VLAN stripping for TEMAC 0	C_TEMAC0_TXVLAN_STRP	1 = Tx VLAN stripping used 0 = Tx VLAN stripping unused	0	integer
Receive VLAN stripping for TEMAC 0	C_TEMAC0_RXVLAN_STRP	1 = Rx VLAN stripping used 0 = Rx VLAN stripping unused	0	integer

Table 4: **XPS_LL_TEMAC Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
Transmit VLAN stripping for TEMAC 1	C_TEMAC1_TXVLAN_STRP	1 = Tx VLAN stripping used 0 = Tx VLAN stripping unused	0	integer
Receive VLAN stripping for TEMAC 1	C_TEMAC1_RXVLAN_STRP	1 = Rx VLAN stripping used 0 = Rx VLAN stripping unused	0	integer
Extended Multicast address filtering for TEMAC 0	C_TEMAC0_MCAST_EXTEND	1 = Extended multicast filtering used 0 = Extended multicast filtering unused	0	integer
Extended Multicast address filtering for TEMAC 1	C_TEMAC1_MCAST_EXTEND	1 = Extended multicast filtering used 0 = Extended multicast filtering unused	0	integer
Statistic gathering for TEMAC 0	C_TEMAC0_STATS	1 = Statistics gathering used 0 = Statistics gathering unused	0	integer
Statistic gathering for TEMAC 1	C_TEMAC1_STATS	1 = Statistics gathering used 0 = Statistics gathering unused	0	integer
Ethernet Audio Video Bridging (AVB) mode for TEMAC 0	C_TEMAC0_AVB	1 = Ethernet AVB mode used 0 = Ethernet AVB mode unused	0	integer

Table 4: **XPS_LL_TEMAC Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
Ethernet Audio Video Bridging 1AVB) mode for TEMAC 0	C_TEMAC1_AVB	1 = Ethernet AVB mode used 0 = Ethernet AVB mode unused	0	integer

1. C_BASEADDR must start on an address boundary that is an integer multiple of 524,288 (512K). For example, valid settings are 0x00000000, 0x00080000, or 0x00180000 etc
2. The default value will insure that the actual value is set, i.e., if the value is not set, a compiler error will be generated. The address range must be at least 0x00080000.
3. C_HIGHADDR is required to be at least C_BASEADDR + 524,287 in order to provide space for the 32-bit addresses used by the registers and memory. For example: C_BASEADDR = 0x00000000, C_HIGHADDR = 0x0007FFFF.
4. These parameters are calculated and automatically assigned by the EDK XPS tools during the system creation process
5. For some combinations of PHY interfaces and device families, IDELAY primitives are used by the xps_ll_temac to help align the receive data with the receive clock. When IDELAY primitives are used, a IDELAYCTRL primitive is also required. The IDELAYCTRL primitive(s) must be located in the proper area in the silicon in order for it to be effective and this is accomplished by adding constraints to the ucf-file. The method for setting the LOC constraint(s) is to use the C_IDELAYCTRL_LOC parameter. This parameter when properly set will generate constraints in the xps_ll_temac core ucf-file. Note that if the LOC constraints are set in the system top-level ucf-file, then this parameter has no effect because the constraints in the system top-level ucf-file override those in lower level ucf-files. The syntax of the parameter value is IDELAYCTRL_XNYM where N and M are coordinates and multiple entries are concatenated by - (i.e, dash). The following is an example of how the parameter might be set in the MHS file. The X and Y values will be different for each implementation. Please refer to the device family User Guide for more information on selecting the correct IDELAY Controller location.
6. The MII supports 10 Mb/S and 100 Mb/S Ethernet speeds. GMII, RGMII, and SGMII support 10 Mb/S, 100 Mb/S, and 1000 Mb/S Ethernet speeds. 1000 BASE-X supports 1000 Mb/S. All PHY_TYPE values support full-duplex only (half-duplex is not supported). Not all PHY types are supported for all TEMAC types. Please refer to Table 1.
7. The value “00000” is a broadcast PHY address and should not be used to avoid contention between the internal HARD_TEMAC PHYs and the external PHY(s).
8. The maximum frame size must not exceed the memory size - 24 bytes. For a memory size of 4096, the maximum frame size is 4072 (4096 - 24).

Allowable Parameter Combinations

Please refer to Table 1, Table 2, and Figure 2 for parameter combination restrictions.

Parameter - Port Dependencies

Table 5: **XPS_LL_TEMAC Parameter-Port Dependencies**

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G1	C_TEMAC1_ENABLED	G2 - G15		If C_TEMAC1_ENABLED is "1" then G2 through G15 values will be used. If C_TEMAC1_ENABLED is "0" then the values of G2 through G15 are ignored.
G2	C_TEMAC1_PHYADDR		G1	
G3	C_TEMAC1_TXFIFO		G1	
G4	C_TEMAC1_RXFIFO		G1	
G5	C_TEMAC1_TXCSUM		G1	
G6	C_TEMAC1_RXCSUM		G1	
G7	C_TEMAC1_TXVLAN_TAG		G1	
G8	C_TEMAC1_RXVLAN_TAG		G1	
G9	C_TEMAC1_TXVLAN_TRAN		G1	
G10	C_TEMAC1_RXVLAN_TRAN		G1	
G11	C_TEMAC1_TXVLAN_STRP		G1	
G12	C_TEMAC1_RXVLAN_STRP		G1	
G13	C_TEMAC1_MCAST_EXTEND		G1	
G14	C_TEMAC1_STATS		G1	
G15	C_TEMAC1_AVB		G1	

Memory and Register Descriptions

The XPS_LL_TEMAC contains memory and addressable registers for read/write operations as shown in Table 6, Table 7, and Table 8 and as shown in Figure 3 (The internal PHY registers will be discussed in greater detail later in this document). The memory map is divided into three types:

1. Memory and registers located in soft logic which are directly addressable via the PLB bus (referred to as memory and soft registers).
2. Registers located in the Hard Silicon TEMAC or the soft TEMAC component which are directly addressable via the PLB bus (referred to as TEMAC direct registers). Three of the four registers (MSW, LSW, CTL) are shared between the two Ethernet interfaces but are accessible from separate addresses for each Ethernet interface. For example, The CTL register is accessible from PLB baseaddr offset 0x028 and also from 0X068. There are separate RDY registers for each Ethernet Interface.

3. Registers located in the Hard Silicon TEMAC or the soft TEMAC component which are indirectly addressable, internal or external PHY device registers connected to the MII management interface, all of which are addressed indirectly through the registers of type 2 above (these are referred to as TEMAC indirect registers).

The base address for the directly addressable registers is set in the parameter C_BASEADDR.

Table 6: **PLB Directly Addressable Memory and Soft Registers**

Register Name	PLB Address (offset from C_BASEADDR)	Access
Reset and Address Filter Register TEMAC 0 (RAF0)	0x00000000	Read/Write
Transmit Pause Frame TEMAC 0 (TPF0)	0x00000004	Read/Write
Transmit Inter Frame Gap Adjustment TEMAC 0 (IFGP0)	0x00000008	Read/Write
Interrupt Status Register TEMAC 0 (IS0)	0x0000000C	Read/Write
Interrupt Pending Register TEMAC 0 (IP0)	0x00000010	Read
Interrupt Enable Register TEMAC 0 (IE0)	0x00000014	Read/Write
Transmit VLAN Tag TEMAC 0 (TTAG0)	0x00000018	Read/Write
Receive VLAN Tag TEMAC 0 (RTAG0)	0x0000001C	Read/Write
Unicast Address Word Lower TEMAC 0 (UAWL0)	0x00000030	Read/Write
Unicast Address Word Upper TEMAC 0 (UAWU0)	0x00000034	Read/Write
VLAN TPID TEMAC 0 Word 0 (TPID00)	0x00000038	Read/Write
VLAN TPID TEMAC 0 Word 1 (TPID01)	0x0000003C	Read/Write
Reset and Address Filter Register TEMAC 1 (RAF1)	0x00000040	Read/Write
Transmit Pause Frame TEMAC 1 (TPF1)	0x00000044	Read/Write
Transmit Inter Frame Gap Adjustment TEMAC 1 (IFGP1)	0x00000048	Read/Write
Interrupt Status Register TEMAC 1 (IS1)	0x0000004C	Read/Write
Interrupt Pending Register TEMAC 1 (IP1)	0x00000050	Read
Interrupt Enable Register TEMAC 1 (IE1)	0x00000054	Read/Write
Transmit VLAN Tag TEMAC 1 (TTAG1)	0x00000058	Read/Write
Receive VLAN Tag TEMAC 1 (RTAG1)	0x0000005C	Read/Write
Unicast Address Word Lower TEMAC 1 (UAWL1)	0x00000070	Read/Write
Unicast Address Word Upper TEMAC 1 (UAWU1)	0x00000074	Read/Write
VLAN TPID TEMAC 1 Word 0 (TPID10)	0x00000078	Read/Write
VLAN TPID TEMAC 1 Word 1 (TPID11)	0x0000007C	Read/Write
Statistics Counters TEMAC 0	0x00000200 - 0x000003FF	Read
Transmit VLAN Data Table TEMAC 0	0x00004000 - 0x00007FFF	Read/Write
Receive VLAN Data Table TEMAC 0	0x00008000 - 0x0000BFFF	Read/Write
Reserved	0x00010000 - 0x00013FFF	Read/Write
Multicast Address Table TEMAC 0	0x00020000 - 0x0003FFFF	Read/Write

Table 6: **PLB Directly Addressable Memory and Soft Registers *(Cont'd)***

Register Name	PLB Address (offset from C_BASEADDR)	Access
Statistics Counters TEMAC 1	0x00040200 - 0x000403FF	Read
Transmit VLAN Data Table TEMAC 1	0x00044000 - 0x00047FFF	Read/Write
Receive VLAN Data Table TEMAC 1	0x00048000 - 0x0004BFFF	Read/Write
Reserved	0x00050000 - 0x00053FFF	Read/Write
Multicast Address Table TEMAC 1	0x00060000 - 0x0007FFFF	Read/Write

Table 7: **PLB Directly Addressable TEMAC Registers**

Register Name	PLB Address (offset from C_BASEADDR)	Access
Hard TEMAC 0 MSW Data Register (MSW0)(1)	0x00000020	Read/Write
Hard TEMAC 0 LSW Data Register (LSW0)	0x00000024	Read/Write
Hard TEMAC 0 Control Register (CTL0)	0x00000028	Read/Write
Hard TEMAC 0 Ready Status (RDY0)	0x0000002C	Read/
Hard TEMAC 1 MSW Data Register (MSW1)(1)	0x00000060	Read/Write
Hard TEMAC 1 LSW Data Register (LSW1)	0x00000064	Read/Write
Hard TEMAC 1 Control Register (CTL1)	0x00000068	Read/Write
Hard TEMAC 1 Ready Status (RDY1)	0x0000006C	Read

1. The MSW registers are used for reading from the Multicast Address Table as these reads can be 64-bits wide. All other transactions only use the LSW registers.

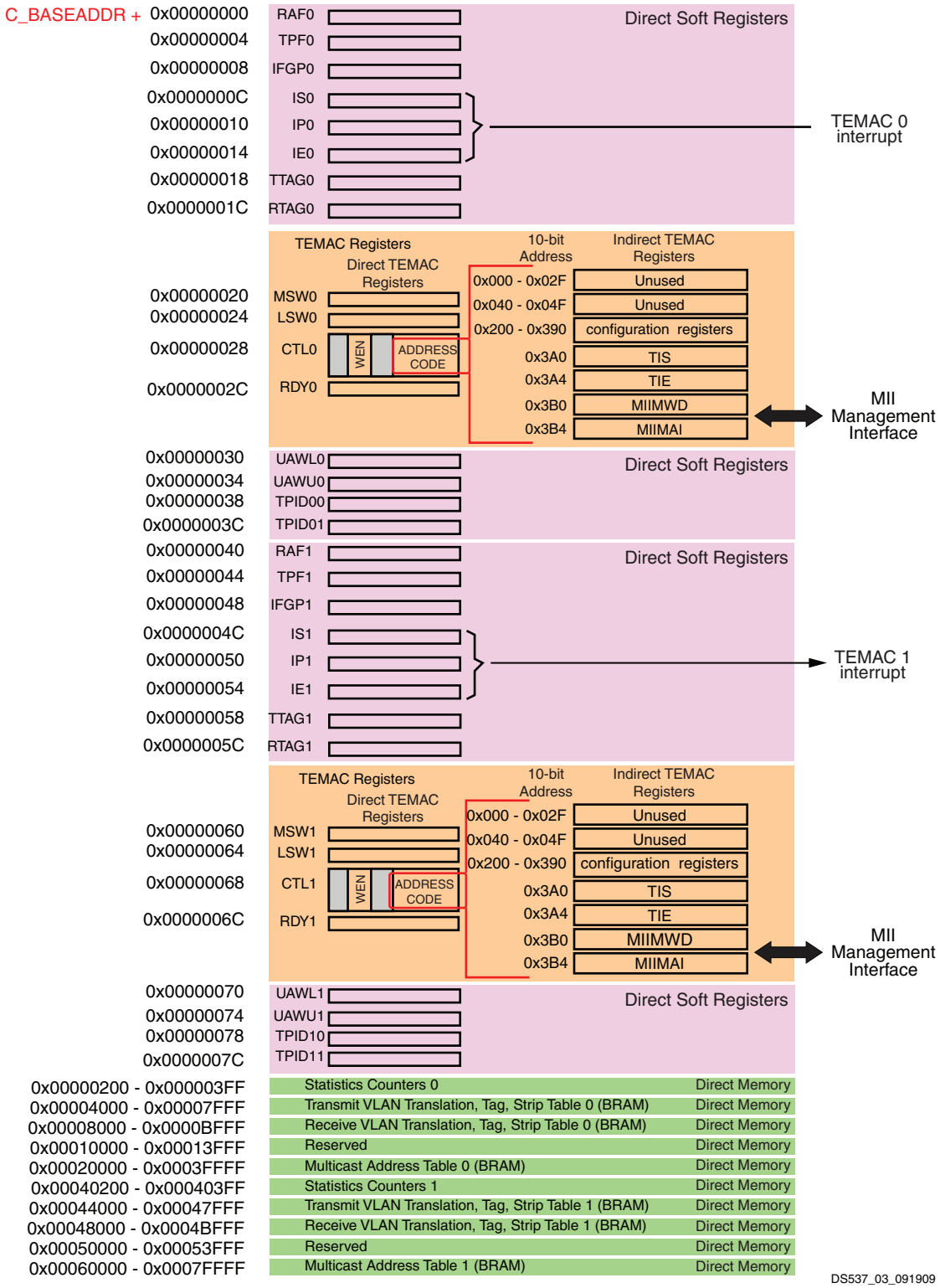

Figure 3: **TEMAC Memory and Registers**

The directly addressable TEMAC registers in Table 7 are used to indirectly access all of the other TEMAC registers (Table 8) and the internal and external PHY registers (via the MII management bus interface).

The indirectly addresses registers for TEMAC interface 0 and interface 1 share the same ADDRESS_CODE field value. The use of CTL0 register or CTL1 register determines which TEMAC interface register is accessed. For example, a ADDRESS_CODE field value of 0x200 is used to access the Receive Configuration Word 0 register. If this address is placed in the CTL0 register then the TEMAC interface 0 register will be accessed. If the address is placed in the CTL1 register then the TEMAC interface 1 register will be accessed.

It is important to note that once an access has been initiated to an indirectly addressed location, the interface will ignore any additional requests for indirect register accesses until the current access is complete. Therefore, it is essential to determine that the current access is complete before issuing a new indirect access command. While some indirect accesses will complete in one clock cycle, others such as accessing PHY registers from the MII Management interface will require many clock cycles.

Determining that an indirect access is complete can be accomplished with two methods using either polling or interrupts.

1. An interrupt indicates that the access is complete. The interrupt HardAcsCmplt must be enabled in the TIE register as well as the IE register. The interrupt must be cleared as described later in this document in the section discussing the interrupt registers.
2. Polling the ready status register (RDY) to determine if the access is complete. The bits in this register are asserted when there is no access in progress. When an access is in progress, a bit corresponding to the type of access is de-asserted. When the access is complete, the bit is re-asserted.

Table 8: **XPS_LL_TEMAC PLB Indirectly Addressable TEMAC Registers**

Register Name	ADDRESS_CODE field of CTL0 or CTL1 register (10 bits)	Access
Unused	0x000 - 0x02F	Read
Unused	0x040 - 0x04F	Read
TEMAC0 or TEMAC1 Receive Configuration Word 0 Register (RCW0)	0x200	Read/Write
TEMAC0 or TEMAC1 Receive Configuration Word 1 Register (RCW1)	0x240	Read/Write
TEMAC0 or TEMAC1 Transmitter Configuration Register (TC)	0x280	Read/Write
TEMAC0 or TEMAC1 Flow Control Configuration Register (FCC)	0x2C0	Read/Write
TEMAC0 or TEMAC1 Ethernet MAC Mode Configuration Register (EMMC)	0x300	Read except bits 30 and 31 which are Read/Write
TEMAC0 or TEMAC1 RGMII/SGMII Configuration Register (PHYC)	0x320	Read
TEMAC0 or TEMAC1 Management Configuration Register (MC)	0x340	Read/Write
TEMAC0 or TEMAC1 Unicast Address Word 0 Register (UAW0)	0x380	Read/Write

Table 8: **XPS_LL_TEMAC PLB Indirectly Addressable TEMAC Registers *(Cont'd)***

Register Name	ADDRESS_CODE field of CTL0 or CTL1 register (10 bits)	Access
TEMAC0 or TEMAC1 Unicast Address Word 1 Register (UAW1)	0x384	Read/Write
TEMAC0 or TEMAC1 Multicast Address Table Access Word 0 Register (MAW0)	0x388	Read/Write
TEMAC0 or TEMAC1 Multicast Address Table Access Word 1 Register (MAW1)	0x38C	Read/Write
TEMAC0 or TEMAC1 Address Filter Mode Register (AFM)	0x390	Read/Write
TEMAC0 or TEMAC1 Interrupt Status Register (TIS)	0x3A0	Read/Write
TEMAC0 or TEMAC1 Interrupt Enable Register (TIE)	0x3A4	Read/Write
TEMAC0 or TEMAC1 MII Management Write Data Register (MIIMWD)	0x3B0	Read/Write
TEMAC0 or TEMAC1 MII Management Access Initiate Register (MIIMAI)	0x3B4	Read/Write

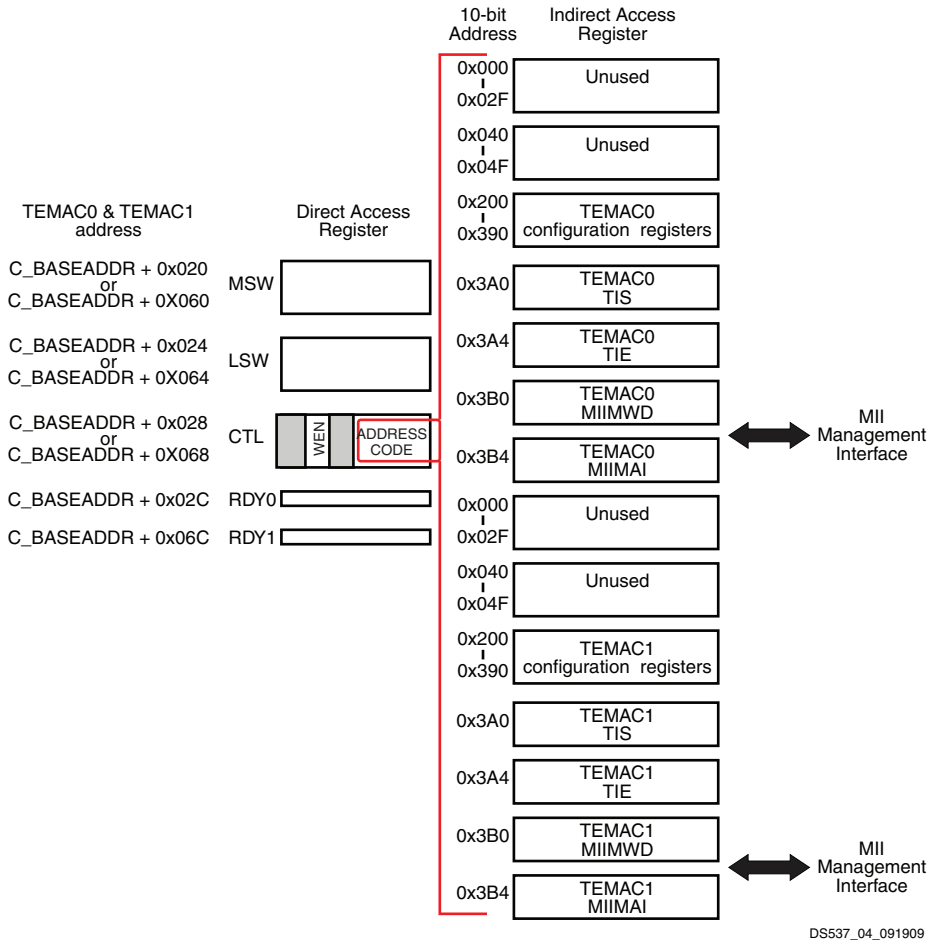

Figure 4: **Direct and Indirect Access TEMAC Registers Address Map**

Directly Addressable Memory and Soft Registers

Reset and Address Filter Registers (RAF0 and RAF1)

The Reset and Address Filter (RAF) Register is shown in Figure 5. This register allows the software to apply a reset to the hard or soft TEMAC component and to block receive multicast and broadcast Ethernet frames. Additional receive address filtering is provided with the indirectly addressable registers in Table 8. A separate RAF register exists for TEMAC interface 0 and TEMAC interface 1.

The multicast reject bit provides a means of blocking receive multicast Ethernet frames without needing to clear out any multicast address values stored in the multicast address table. It also provides a means for allowing more than 4 multicast addresses to be received (the limit of the multicast address table). To accept more than 4 multicast addresses, the AFM register would be set to promiscuous mode and the multicast reject bit of this register set to allow multicast frames. Note that software may also need to filter out additional receive frames with other addresses.

The broadcast reject bit provides the only means for rejecting receive broadcast Ethernet frames.

Due to the design of the TEMAC component, setting the reset bit in either RAF register will reset all (both interfaces) of the TEMAC component.

As additional functionality was added to the core, this register became the convenient home for new bits to control those new functions. Care has been take to minimize the effect of these new bits on existing applications by ensuring that the default values of these bits disable new functionality. This will ensure that when applications do not use the new bits, the core will operate the way it did previously.

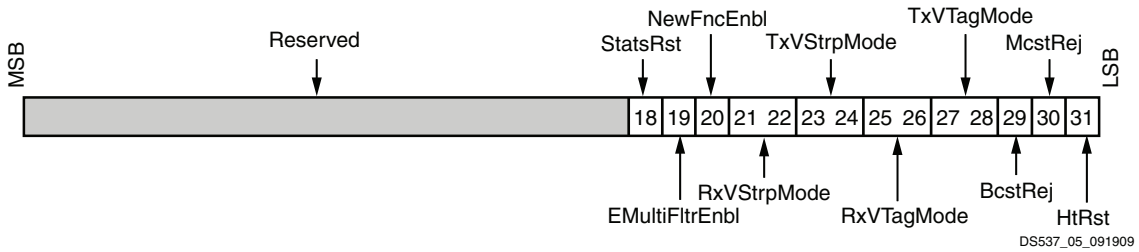

Figure 5: **Reset and Address Filter Registers (offset 0x000 and 0x040)**

Table 9 shows the Reset and Address Filter Register bit definitions.

Table 9: **Reset and Address Filter Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	HtRst	Read/Write	0	**Hard TEMAC Reset.** This bit provides a means for resetting the TEMAC component. This bit is self clearing. 0 - normal operation, TEMAC not reset 1 - initiate a reset of the TEMAC (both Ethernet interfaces)
30	McstRej	Read/Write	0	**Reject Receive Multicast Destination Address.** This bit provides a means for accepting or rejecting multicast Ethernet frames. 0 - accept receive multicast destination address Ethernet frames that meet address filtering specified in AFM register an/or the multicast address table 1 - reject all receive multicast destination address Ethernet frames regardless of AFM register and multicast address table
29	BcstRej	Read/Write	0	**Reject Receive Broadcast Destination Address.** This bit provides a means for accepting or rejecting broadcast Ethernet frames. 0 - accept receive broadcast destination address Ethernet frames 1 - reject all receive broadcast destination address Ethernet frames. This is the only method available for blocking broadcast Ethernet frames

Table 9: **Reset and Address Filter Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
27-28	TxVTagMode	Read/Write	00	**Transmit VLAN Tag Mode.** These bits select the operation mode for transmit VLAN tagging and are only used when C_TEMACx_TXVLAN_TAG = 1. The VLAN tag that is added is from the TTAGx register. Valid VLAN TPID values must be initialized in the TPIDx0 and TPIDx1 registers. For mode 11, the Transmit VLAN data table must be initialized. Please refer to the VLAN section of this document for more details. 00 - No VLAN tags will be added to transmit frames 01 - VLAN tags will be added to all transmit frames 10 - VLAN tags will be added to all transmit frames that already have a VLAN tag 11 - VLAN tags will be added to select transmit frames that already have VLAN tags
25-26	RxVTagMode	Read/Write	00	**Receive VLAN Tag Mode.** These bits select the operation mode for receive VLAN tagging and are only used when C_TEMACx_RXVLAN_TAG = 1. The VLAN tag that is added is from the RTAGx register. Valid VLAN TPID values must be initialized in the TPIDx0 and TPIDx1 registers. For mode 11, the Receive VLAN data table must be initialized. Please refer to the VLAN section of this document for more details. 00 - No VLAN tags will be added to receive frames 01 - VLAN tags will be added to all receive frames 10 - VLAN tags will be added to all receive frames that already have a VLAN tag 11 - VLAN tags will be added to select receive frames that already have VLAN tags
23-24	TxVStrpMode	Read/Write	00	**Transmit VLAN Strip Mode.** These bits select the operation mode for transmit VLAN stripping and are only used when C_TEMACx_TXVLAN_STRP = 1. Valid VLAN TPID values must be initialized in the TPIDx0 and TPIDx1 registers. For mode 11, the Transmit VLAN data table must be initialized. Please refer to the VLAN section of this document for more details. 00 - No VLAN tags will be stripped from transmit frames 01 - One VLAN tag will be stripped from all transmit frames that have VLAN tags 10 - Reserved 11 - One VLAN tag will be stripped from select transmit frames that already have VLAN tags
21-22	RxVStrpMode	Read/Write	00	**Receive VLAN Strip Mode.** These bits select the operation mode for receive VLAN stripping and are only used when C_TEMACx_RXVLAN_STRP = 1. Valid VLAN TPID values must be initialized in the TPIDx0 and TPIDx1 registers. For mode 11, the Receive VLAN data table must be initialized. Please refer to the VLAN section of this document for more details. 00 - No VLAN tags will be stripped from receive frames 01 - One VLAN tag will be stripped from all receive frames that have VLAN tags 10 - Reserved 11 - One VLAN tag will be stripped from select receive frames that already have VLAN tags

Table 9: **Reset and Address Filter Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
20	NewFncEnbl	Read/Write	0	**New Functions Enable.** This bit provides a simple way to disable new functions that have been added in this version. This includes the VLAN tagging, VLAN stripping, VLAN translation, and extended multicast filtering. Enabling the new functions will only affect operation if the functions have been added to the design using the appropriate parameters at build-time. 0 - disable new functions 1 - enable new functions if present
19	EMultiFltrEnbl	Read/Write	0	**Enhanced Multicast Filter Enable.** This bit provides a simple way to disable the new enhanced multicast filtering if present. This is necessary if promiscuous address reception mode is desired or if use of the built-in 4 TEMAC multicast address registers is required when the core includes the enhanced multicast address filtering function enabled at build time by the C_TEMACx_MCAST_EXTEND parameters. Please refer to the Enhanced Multicast Filtering section of this document for more details. 0 - disable enhanced multicast address filtering mode 1 - enable enhanced multicast address filtering mode if present
18	StatsRst	Read/Write	0	**Statistics Counters Reset.** This bit provides a means for resetting the statistics counters if present. This bit is self clearing. 0 - normal operation, statistics counters not reset 1 - initiate a reset of the statistics counters
0 - 17	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

Transmit Pause Frame Registers (TPF0 and RPF1)

The Transmit Pause Frame TEMAC 0 Register is shown in Figure 6. This register provides a value of pause when enabled by the FCC register (page 59). When enabled, the Ethernet will transmit a pause frame whenever this register is written. Pause values are defined in units of pause quanta which are defined as 512 bit times for the current transmission speed. Therefore, pause times may have values ranging from 0 to 65,535 * 512 bit times. A separate TPF register exists for TEMAC interface 0 and TEMAC interface 1.

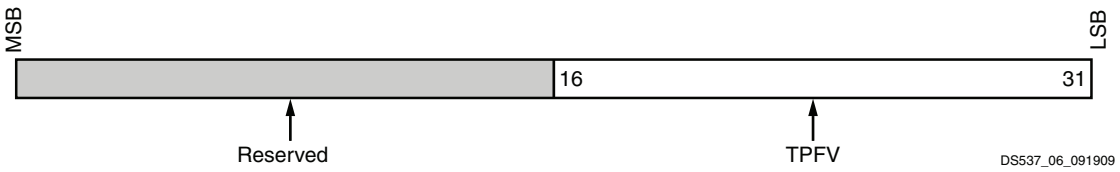

Figure 6: **Transmit Pause Frame Registers (offset 0x004 and 0x044)**

Table 10 shows the Transmit Pause Frame Register bit definitions.

Table 10: **Transmit Pause Frame register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
16 - 31	TPFV	Read/Write	0x0	**Transmit Pause Frame Value.** These bits denote the value of the transmit pause frame pause time in units of 512 bit times. If enabled by the FCC register, writing a value into this register initiates the transmission of a single pause frame with the pause value defined in this field.
0 - 15	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

Transmit Inter Frame Gap Adjustment Registers (IFGP0 and IFGP1)

The Transmit Inter Frame Gap Adjustment Register is shown in Figure 7. This register provides a duration value of Inter Frame Gap when enabled by the TC register (page 58). When enabled, the TEMAC will use the value of this register to extend the Inter Frame Gap beyond the minimum of 12 idle cycles which is 96-bit times on the Ethernet Interface. A separate IFGP register exists for TEMAC interface 0 and TEMAC interface 1.

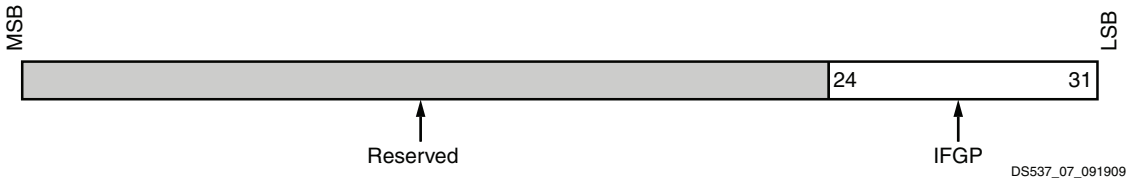

Figure 7: **Transmit Inter Frame Gap Adjustment Registers (offset 0x008 and 0x048)**

Table 11 shows the Transmit Inter Frame Gap Adjustment Register bit definitions.

Table 11: **Transmit Inter Frame Gap Adjustment Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
24 - 31	IFGP0	Read/Write	0x0	**Transmit Inter Frame Gap Adjustment Value.** This 8-bit value can be used along with the Inter Frame Gap Adjustment Enable bit of the Transmit Configuration Register (See "TEMAC Control Register Bit Definitions" on page 52) to increase the Transmit Inter Frame Gap. This value is the width of the IFG in idle cycles. Each idle cycle is 8 bit times on the Ethernet interface. The minimum IFG time is 12 idle cycles which is 96 bit-times. If this field value is less than 12 or if IFGP adjustment is disabled in the Transmit Configuration register, an IFGP of 12 idle cycles (96-bit times) will be used.
0 - 23	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

Interrupt Status Registers (IS0 and IS1)

The Interrupt Status Register is shown in Figure 8. This register combined with the IE, IP, TIS, and TIE registers define the interrupt interface of the XPS_LL_TEMAC. The Interrupt Status register uses one bit to represent each XPS_LL_TEMAC internal interruptible condition. One of these interruptible conditions, Hard register Access Complete (HardAcsCmplt), comes from the TEMAC component and is

further defined and enabled by the TIS and TIE registers which will be described later in this document. A separate IS register exists for TEMAC interface 0 and TEMAC interface 1.

Once an interruptible condition occurs, it will be captured in this register (represented as the corresponding bit being set to 1) even if the condition goes away. The latched interruptible condition is cleared by writing a 1 to that bit location. Writing a 1 to a bit location that is 0 has no effect. Likewise, writing a 0 to a bit location that is 1 has no effect. Multiple bits may be cleared in a single write.

For any bit set in the Interrupt Status Register, a corresponding bit must be set in the Interrupt Enable Register for the same bit position to be set in the Interrupt pending register. Whenever any bit are set in the Interrupt Pending Register, the TemacIntc_Irpt signal is driven active high out of the XPS_LL_TEMAC. Figure 9 shows the structure of the interrupt registers.

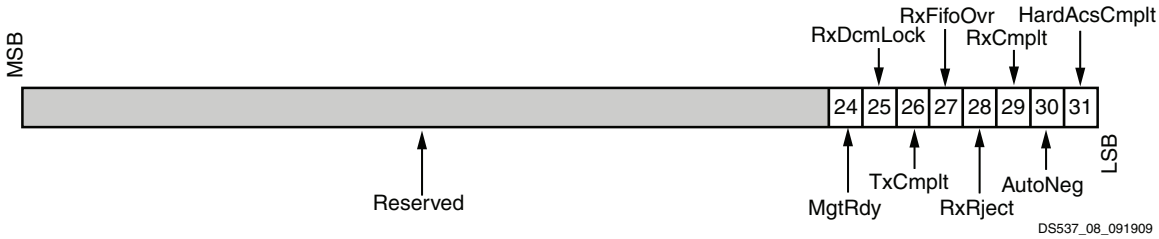

Figure 8: **Interrupt Status Registers (offset 0x00C and 0x04C)**

Table 12 shows the Interrupt Status Register bit definitions.

Table 12: **Interrupt Status Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	HardAcsCmplt	Read/Write	0	**Hard register Access Complete.** This bit indicates that an access of the TEMAC component has completed. 0 - Hard register access is not complete 1 - Hard register access is complete
30	AutoNeg	Read/Write	0	**Auto Negotiation Complete.** This bit indicates that auto negotiation of the SGMII or 1000 Base-X interface has completed. 0 - auto negotiation not complete 1 - auto negotiation complete
29	RxCmplt	Read/Write	0	**Receive Complete.** This bit indicates that a packet was successfully received. 0 - no frame received 1 - frame received
28	RxRject(1)	Read/Write	0	**Receive Frame Rejected.** This bit indicates that a receive frame was rejected. 0 - no receive frame rejected 1 - receive frame was rejected
27	RxFifoOvr	Read/Write	0	**Receive FIFO Overrun.** This bit indicates that the receive FIFO overflowed while receiving an Ethernet frame. 0 - normal operation, no overflow occurred 1 - receive FIFO overflow occurred and data was lost

Table 12: **Interrupt Status Register Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
26	TxCmplt	Read/Write	0	**Transmit Complete.** This bit indicates that a frame was successfully transmitted. 0 - no frame transmitted 1 - frame transmitted
25	RxDcmLock	Read/Write	0	**Receive DCM Lock.** When using the soft TEMAC in a Spartan-3 device at 1000 Mbs, a DCM is used to phase-shift the PHY receive clock to align it with the PHY receive data. This DCM requires a time period to lock to the PHY receive clock whenever a reset or Ethernet speed change is made. While the DCM is unlocked, the TEMAC is not able to receive Ethernet frames. This interrupt bit will indicate when the DCM has locked to the PHY receive clock and normal Ethernet operation can take place. This bit will always be one when using the hard TEMAC implementations or when using the soft TEMAC in a device other than Spartan-3. 0 - Rx DCM not locked 1 - Rx DCM Locked
24	MgtRdy	Read/Write	0 / 1 (2)	**MGT Ready.** This bit will indicate if the TEMAC is out of reset and ready for use. In systems that use an MGT, this bit will go to '1' when the MGT is ready to use. Prior to that time, access of TEMAC indirect access registers will not complete and the core will not operate. In systems that do not use an MGT, this signal will go to '1' immediately after reset. 0 - MGT / TEMAC not ready 1 - MGT / TEMAC ready
0 - 23	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

1. Please refer to Figure 50 on page 87 for conditions that will cause the receive frame reject interrupt to occur. The receive frame reject interrupt will occur for any of the following reasons:
   A. The frame does not meet the Ethernet frame requirements as determined by the hard TEMAC core (bad FCS, bad length, etc).
   B. In addition to the frame being good but not meeting the destination address filtering by the hard TEMAC, the frame also does not match one of the 4 multicast table entries, it is not a broadcast frame, it does not match the unicast address register, and the Hard TEMAC core is not in promiscuous mode.
   C. The core was built to support extended multicast address filtering (C_TEMACx_MCAST_EXTEND=1), but the hard TEMAC core is not in promiscuous mode.
   D. The frame is good and meets the destination address filtering by the hard TEMAC but it is a multicast frame and the multicast reject bit is set in the soft RAF register.
   E. The frame is good and meets the destination address filtering by the hard TEMAC but it is a broadcast frame and the broadcast reject bit is set in the soft RAF register.
2. This bit will reset to '0' but may change to '1' immediately after reset is removed. This bit may remain at '0' for some time in systems that are using MGTs when the MGTs are not yet ready for use.

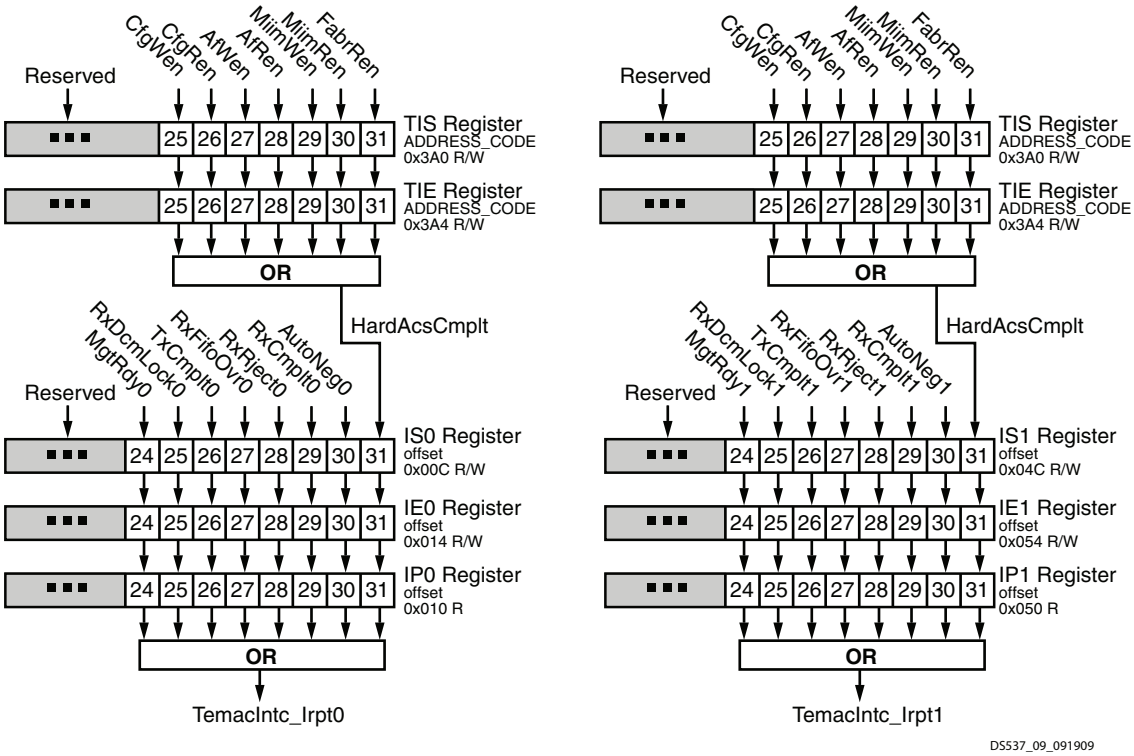

Figure 9: **XPS_LL_TEMAC Interrupt Structure**

Interrupt Pending Registers (IP0 and IP1)

The Interrupt Pending Register is shown in Figure 10. This register combined with the IS, IE, TIS, and TIE registers define the interrupt interface of the XPS_LL_TEMAC. The Interrupt Pending register uses one bit to represent each XPS_LL_TEMAC internal interruptible condition that is represented in the Interrupt Status Register.

If one or more interrupt is latched in the Interrupt Status Register and corresponding enable bits are set in the Interrupt Enable Register, then the corresponding bit is set in the Interrupt Pending Register. If one or more bits is set in the Interrupt Pending register then the TemacIntc_Irpt signal is driven active high out of the XPS_LL_TEMAC. A separate IP register exists for TEMAC interface 0 and TEMAC interface 1.

The Interrupt Pending Register always represents the state of the Interrupt Status register bitwise ANDed with the IE register. The Interrupt Pending Register is read only. In order to clear a bit in the Interrupt Pending Register, either the corresponding bit must be cleared in either the Interrupt Status Register or the Interrupt Enable Register.

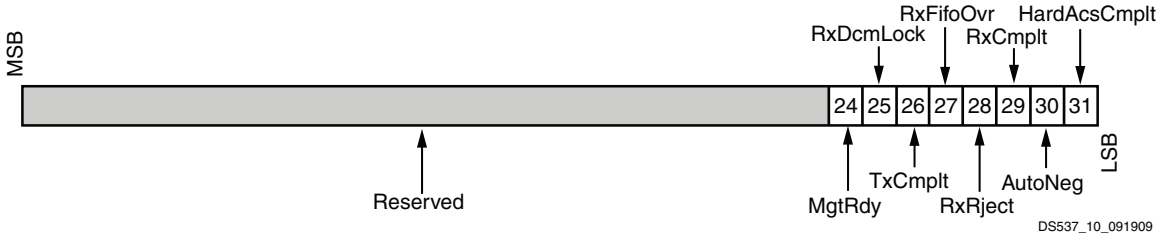

Figure 10: **Interrupt Pending Registers (offset 0x010 and 0x050)**

Table 13 shows the Interrupt Pending Register bit definitions.

Table 13: **Interrupt Pending Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	HardAcsCmplt	Read/Write	0	**Hard register Access Complete.** This bit indicates that an access of the TEMAC component has completed. 0 - Hard register access is not complete 1 - Hard register access is complete
30	AutoNeg	Read	0	**Auto Negotiation Complete Ethernet.** This bit indicates that auto negotiation of the SGMII or 1000 Base-X interface has completed. 0 - auto negotiation no complete 1 - auto negotiation complete
29	RxCmplt	Read	0	**Receive Complete.** This bit indicates that a packet was successfully received. 0 - no frame received 1 - frame received
28	RxRject	Read	0	**Receive Frame Rejected.** This bit indicates that a receive frame was rejected. 0 - no receive frame rejected 1 - receive frame was rejected
27	RxFifoOvr	Read	0	**Receive FIFO Overrun.** This bit indicates that the receive FIFOs overflowed while receiving an Ethernet frame. 0 - normal operation, no overflow occurred 1 - receive FIFO overflow occurred and data was lost
26	TxCmplt	Read	0	**Transmit Complete.** This bit indicates that a frame was successfully transmitted. 0 - no frame transmitted 1 - frame transmitted
25	RxDcmLock	Read	0	**Receive DCM Lock.** When using the soft TEMAC in a Spartan-3 device at 1000 Mbs, a DCM is used to phase-shift the PHY receive clock to align it with the PHY receive data. This DCM requires a time period to lock to the PHY receive clock whenever a reset or Ethernet speed change is made. While the DCM is unlocked, the TEMAC is not able to receive Ethernet frames. This interrupt bit will indicate when the DCM has locked to the PHY receive clock and normal Ethernet operation can take place. This bit will always be one when using the hard TEMAC implementations or when using the soft TEMAC in a device other than Spartan-3. 0 - Rx DCM not locked 1 - Rx DCM Locked

Table 13: **Interrupt Pending Register Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
24	MgtRdy	Read	0	**MGT Ready.** This bit will indicate if the TEMAC is out of reset and ready for use. In systems that use an MGT, this bit will go to '1' when the MGT is ready to use. Prior to that time, access of TEMAC indirect access registers will not complete and the core will not operate. In systems that do not use an MGT, this signal will go to '1' immediately after reset. 0 - MGT / TEMAC not ready 1 - MGT / TEMAC ready
0 - 23	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

Interrupt Enable Registers (IE0 and IE1)

The Interrupt Enable Register is shown in Figure 11. This register combined with the IS, IP, TIS, and TIE registers define the interrupt interface of the XPS_LL_TEMAC. The Interrupt Enable register uses one bit to represent each XPS_LL_TEMAC internal interruptible condition represented in the Interrupt Status Register. A separate IE register exists for TEMAC interface 0 and TEMAC interface 1.

Each bit set in the Interrupt Enable Register allows an interruptible condition bit in the Interrupt Status Register to pass through to the Interrupt Pending Register.

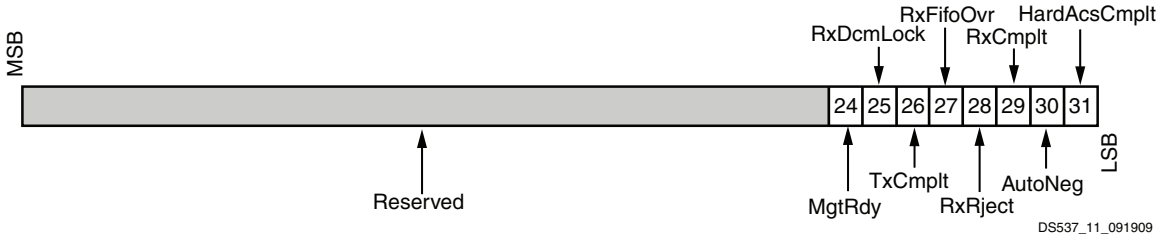

Figure 11: **Interrupt Enable Registers (offset 0x014 and 0x054)**

Table 14 shows the Interrupt Enable Register bit definitions.

Table 14: **Interrupt Enable Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	HardAcsCmplt	Read/Write	0	**Hard register Access Complete.** This bit indicates that an access of the TEMAC component has completed. 0 - Hard register access is not complete 1 - Hard register access is complete
30	AutoNeg	Read/Write	0	**Auto Negotiation Complete.** This bit indicates that auto negotiation of the SGMII or 1000 Base-X interface has completed. 0 - auto negotiation complete interrupt disabled 1 - auto negotiation complete interrupt enabled
29	RxCmplt	Read/Write	0	**Receive Complete.** This bit indicates that a packet was successfully received. 0 - frame received interrupt disabled 1 - frame received interrupt enabled

Table 14: **Interrupt Enable Register Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
28	RxRject	Read/Write	0	**Receive Frame Rejected.** This bit indicates that a receive frame was rejected. 0 - receive frame was rejected interrupt disabled 1 - receive frame was rejected interrupt enabled
27	RxFifoOvr	Read/Write	0	**Receive FIFO Overrun.** This bit indicates that the receive FIFOs overflowed while receiving an Ethernet frame. 0 - receive FIFO overflow occurred interrupt disabled 1 - receive FIFO overflow occurred interrupt enabled
26	TxCmplt	Read/Write	0	**Transmit Complete.** This bit indicates that a frame was successfully transmitted. 0 - frame transmitted interrupt disabled 1 - frame transmitted interrupt enabled
25	RxDcmLock	Read/Write	0	**Receive DCM Lock.** When using the soft TEMAC in a Spartan-3 device at 1000 Mbs, a DCM is used to phase-shift the PHY receive clock to align it with the PHY receive data. This DCM requires a time period to lock to the PHY receive clock whenever a reset or Ethernet speed change is made. While the DCM is unlocked, the TEMAC is not able to receive Ethernet frames. This interrupt bit will indicate when the DCM has locked to the PHY receive clock and normal Ethernet operation can take place. This bit will always be one when using the hard TEMAC implementations or when using the soft TEMAC in a device other than Spartan-3. 0 - Rx DCM not locked 1 - Rx DCM Locked
24	MgtRdy	Read	0	**MGT Ready.** This bit will indicate if the TEMAC is out of reset and ready for use. In systems that use an MGT, this bit will go to '1' when the MGT is ready to use. Prior to that time, access of TEMAC indirect access registers will not complete and the core will not operate. In systems that do not use an MGT, this signal will go to '1' immediately after reset. 0 - MGT / TEMAC not ready 1 - MGT / TEMAC ready
0 - 23	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

Transmit VLAN Tag Register (TTAG0 and TTAG1)

The Transmit VLAN Tag Register is shown in Figure 12. This register is only used when the VLAN tagging is included in the core at build-time (C_TEMACx_TXVLAN_TAG = 1). When a VLAN tag is added to a transmit frame, this is the value that is added to the frame right after the source address field. Please see the section on VLAN functions ("Extended VLAN Support" on page 93) for more information about how VLAN tagging is performed.

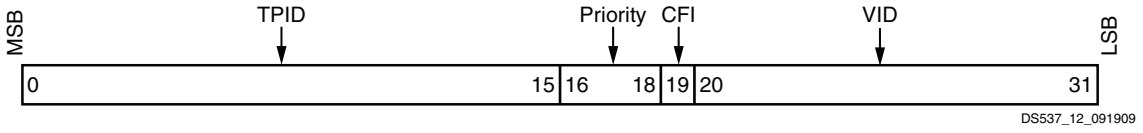

Figure 12: **Transmit VLAN Tag Register (offset 0x018 and 0x058)**

Table 15 shows the Transmit VLAN Tag Register bit definitions.

Table 15: **Transmit VLAN Tag register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
20 - 31	VID	Read/Write	0x0	**VLAN identifier.** Uniquely identifies the VLAN to which the frame belongs
19	CFI	Read/Write	0	Canonical Format Indicator.
16 - 18	Priority	Read/Write	0x0	User Priority.
0 - 15	TPID	Read/Write	0x0	Tag Protocol Identifier.

Receive VLAN Tag Register (RTAG0 and RTAG1)

The Receive VLAN Tag Register is shown in Figure 13. This register is only used when the VLAN tagging is included in the core at build-time (C_TEMACx_RXVLAN_TAG = 1). When a VLAN tag is added to a receive frame, this is the value that is added to the frame right after the source address field. Please see the section on VLAN functions ("Extended VLAN Support" on page 93) for more information about how VLAN tagging is performed.

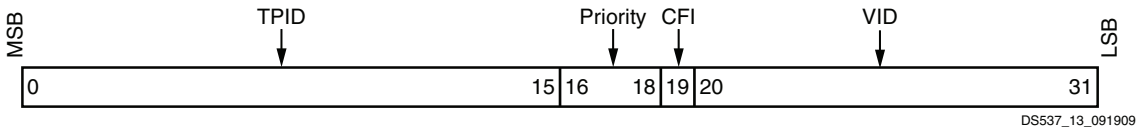

Figure 13: **Receive VLAN Tag Register (offset 0x01C and 0x05C)**

Table 16 shows the Receive VLAN Tag Register bit definitions.

Table 16: **Receive VLAN Tag register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
20 - 31	VID	Read/Write	0x0	**VLAN identifier.** Uniquely identifies the VLAN to which the frame belongs
19	CFI	Read/Write	0	Canonical Format Indicator.
16 - 18	Priority	Read/Write	0x0	User Priority.
0 - 15	TPID	Read/Write	0x0	Tag Protocol Identifier.

Unicast Address Word Lower Register (UAWL0 and UAWL1)

The Unicast Address Word Lower Register is shown in Figure 14. This register and the following register are **only used when extended multicast filtering is included** in the core at build-time (C_TEMACx_MCAST_EXTEND = 1) and is enabled. These registers should not be confused with the UAW0 and UAW1 registers which are indirect access registers inside the TEMAC core which are **only used when extended multicast filtering is excluded in the core at build-time or is disabled**. When using extended multicast filtering, the TEMAC core must be placed in promiscuous address filtering mode. This register allows filtering of unicast frames not matching the address stored in these registers. Please see the section on Extended Multicast Filtering for more information ("Extended Multicast Address Filtering Mode" on page 87).

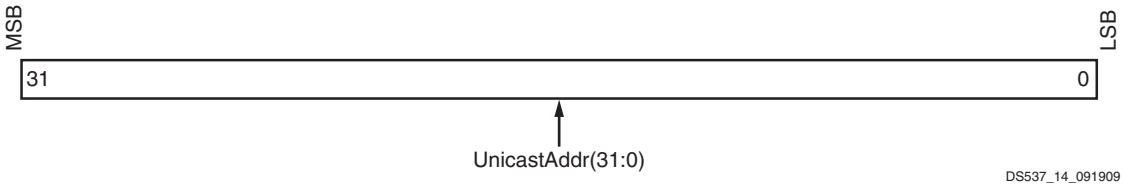

Figure 14: **Unicast Address Word Lower Register (offset 0x030 and 0x070)**

Table 17 shows the Unicast Address Word Lower Registers bit definitions.

Table 17: **Unicast Address Word Lower Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 31	UnicastAddr	Read/Write	0x00000000	**Unicast Address (31:0).** This address is used to match against the destination address of any received frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA.

Unicast Address Word Upper Register (UAWU0 and UAWU1)

The Unicast Address Word Upper Register is shown in Figure 15. This register and the previous register are only used when extended multicast filtering is included in the core at build-time (C_TEMACx_MCAST_EXTEND = 1). When using extended multicast filtering, the TEMAC core must be placed in promiscuous address filtering mode. This register allows filtering of unicast frames not matching the address stored in these registers. Please see the section on Extended Multicast Filtering for more information ("Extended Multicast Address Filtering Mode" on page 87).

Figure 15: **Unicast Address Word Upper Register (offset 0x034 and 0x074)**

Table 18 shows the Unicast Address Word Upper Registers bit definitions.

Table 18: **Unicast Address Word Upper Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
16 - 31	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.
0 - 15	UnicastAddr	Read/Write	0x00000000	**Unicast Address (47:32).** This address is used to match against the destination address of any received frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA.

VLAN TPID Word 0 Register (TPID00 and TPID10)

The VLAN TPID Word 0 Register is shown in Figure 16. This register is only used when transmit and/or receive VLAN functions are included in the core at build-time (C_TEMACx_TXVLAN_TAG = 1 and/or C_TEMACx_RXVLAN_TAG = 1 and/or C_TEMACx_TXVLAN_STRP= 1 and/or C_TEMACx_RXVLAN_STRP= 1 and/or C_TEMACx_TXVLAN_TRAN = 1 and/or C_TEMACx_RXVLAN_TRAN = 1).

This register and the following register allow 4 TPID values be specified for recognizing VLAN frames for both the transmit and receive paths. The most common values for VLAN TPID are 0x8100, 0x9100, 0x9200, 0x88A8. Please see the section on VLAN functions ("Extended VLAN Support" on page 93) for more information about extended VLAN functions.

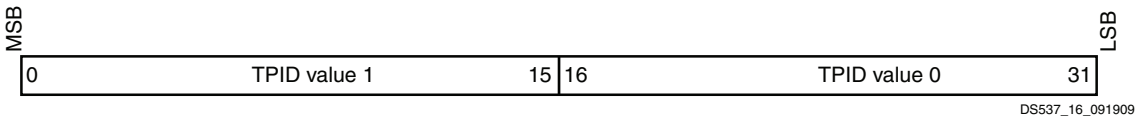

Figure 16: **VLAN TPID Word 0 Register (offset 0x038 and 0x078)**

Table 19 shows the VLAN TPID Word 0 Registers bit definitions.

Table 19: **VLAN TPID Word 0 Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
16 - 31	TPID value 0	Read/Write	0x0	**TPID Value 0.** These bits represent one TPID value that will be used for recognizing VLAN frames for both the transmit and receive paths.
0 - 15	TPID value1	Read/Write	0x0	**TPID Value 1.** These bits represent one TPID value that will be used for recognizing VLAN frames for both the transmit and receive paths.

VLAN TPID Word 1 Register (TPID01 and TPID11)

The VLAN TPID Word 1 Register is shown in Figure 17. This register is only used when transmit and/or receive VLAN functions are included in the core at build-time (C_TEMACx_TXVLAN_TAG = 1 and/or C_TEMACx_RXVLAN_TAG = 1 and/or C_TEMACx_TXVLAN_STRP= 1 and/or

C_TEMACx_RXVLAN_STRP= 1 and/or C_TEMACx_TXVLAN_TRAN = 1 and/or C_TEMACx_RXVLAN_TRAN = 1).

This register and the previous register allow 4 TPID values be specified for recognizing VLAN frames for both the transmit and receive paths. The most common values for VLAN TPID are 0x8100, 0x9100, 0x9200, 0x88A8. Please see the section on VLAN functions ("Extended VLAN Support" on page 93) for more information about extended VLAN functions.

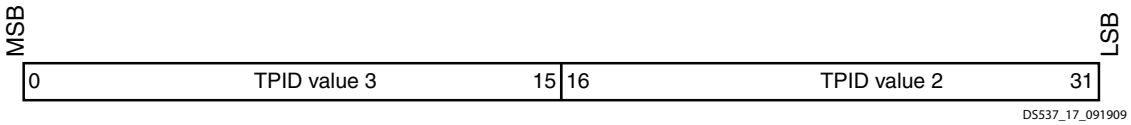

Figure 17: **VLAN TPID Word 1 Register (offset 0x03C and 0x07C)**

Table 20 shows the VLAN TPID Word 1 Registers bit definitions.

Table 20: **VLAN TPID Word 1 Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
16 - 31	TPID value 2	Read/Write	0x0	**TPID Value 2.** These bits represent one TPID value that will be used for recognizing VLAN frames for both the transmit and receive paths.
0 - 15	TPID value3	Read/Write	0x0	**TPID Value 3.** These bits represent one TPID value that will be used for recognizing VLAN frames for both the transmit and receive paths.

Multicast Address Table (0 and 1)

The Multicast Address Table entry is shown in Figure 19. The multicast address table is only present when extended multicast address filtering is selected at build-time (C_TEMACx_MCAST_EXTEND = 1). The purpose of the table is to allow the xps_ll_temac to support reception of frames addressed to many multicast addresses while providing some of the filtering in hardware to off load some of the overhead required for filtering in software.

While a MAC multicast address is defined as any 48 bit MAC address that has bit 0 (LSb) set to 1 (for example 01:00:00:00:00:00), in most cases the MAC multicast address is created from a IP multicast address as shown in Figure 18.

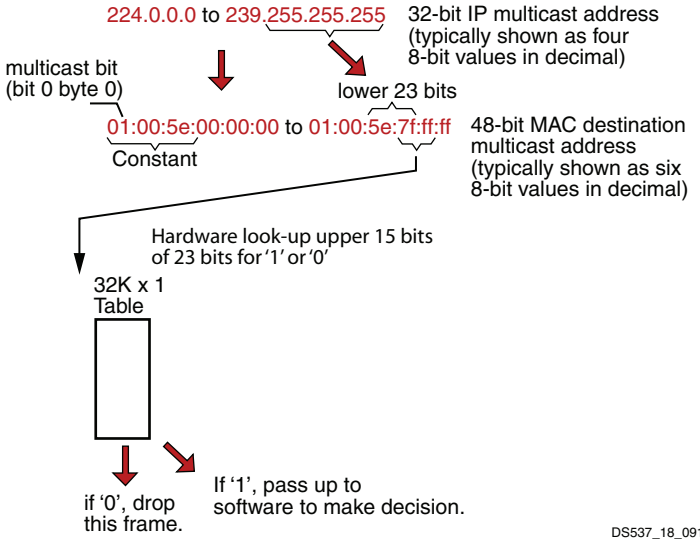

Figure 18: **Mapping IP Multicast Addresses to MAC Multicast Addresses**

When a multicast address frame is received while this extended multicast filtering is enabled, the xps_ll_temac first verifies that the first 24 bits are 01:00:5E and then will use the upper 15 bits of the unique 23 bit MAC multicast address to index this memory. If the associated memory location contains a 1 then the frame is accepted and passed up to software for a comparison on the full 23-bit address. If the memory location is a 0 or the upper 24 bits are not 01:00:5E then the frame is not accepted and it is dropped.

The memory is 1-bit wide but is addressed on 32-bit word boundaries. The memory is 32K deep. This table must be initialized by software via the PLB interface

When using the extended multicast address filtering, the TEMAC must be set to promiscuous mode so that all frames are available for filtering. When doing this the TEMAC no longer checks for a unicast address match. Additional registers (UAWLx and UAWUx) are available to provide unicast address filtering while in this mode.

For builds that have the extended multicast address filtering enabled, promiscuous mode can be achieved by making sure that the TEMAC is in promiscuous mode and by clearing the EMultiFltrEnbl bit (bit 19) in the Reset and Address Filter register (RAF).

Please see the section on Extended Multicast Filtering for more details ("Extended Multicast Address Filtering Mode" on page 87).

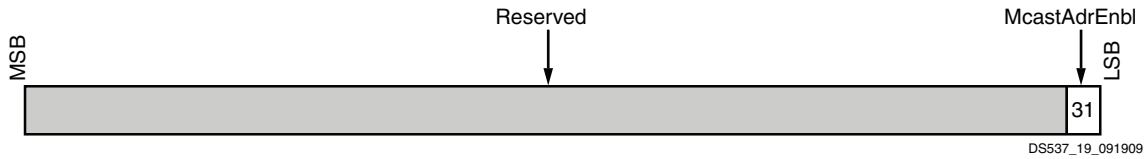

Figure 19: **Multicast Address Table entry (offset 0x20000-0x3FFFF and 0x60000-0x7FFFF)**

Table 21 shows the Multicast Address Table bit definitions.

Table 21: **Multicast Address Table Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	McastAdrEnbl	Read/Write	0	**Multicast Address Enable.** This bit indicates that the received multicast frame with this upper 15 bits of the unique 23-bit MAC multicast address field should be accepted or rejected. 0 - Drop this frame 1 - Accept this frame
0 - 30	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

Transmit VLAN Data Table (0 and 1)

This table is used for data to support transmit VLAN tagging, VLAN stripping, and VLAN translation. The table is always 4K entries deep but the width depends on how many of the VLAN functions are included at build time. VLAN translation requires 12 bits at each location while VLAN stripping and VLAN tagging require 1 bit each at each location.

When all transmit VLAN functions are included, the table is 14 bits wide. If VLAN functions are not included, the bits for those functions will not be present and writes to those bits will have no effect while reads will return zero.

The table may be either 1-bit, 2-bits, 12-bits, 13-bits, or 14-bits wide depending on which features are present. The table must be initialized by software via the PLB and is addressed on 32-bit word boundaries.

The transmit VLAN Table entry with all VLAN functions present is shown in Figure 20 while Figure 21 shows the transmit VLAN Table entry with only the translation field. Note that the bit locations for the functions do not change even when some functions are not used in the build.

Please see the section on VLAN functions for more details ("Extended VLAN Support" on page 93).

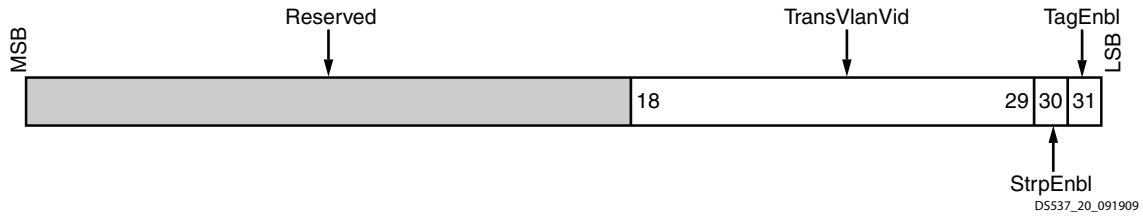

Figure 20: **Transmit VLAN Table entry w/ all fields (offset 0x4000-0x7FFF and 0x44000-0x47FFF)**

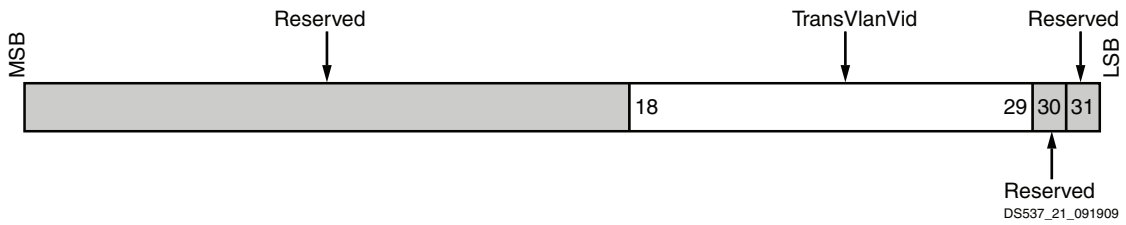

Figure 21: **Transmit VLAN Table entry w/ one field (offset 0x4000-0x7FFF and 0x44000-0x47FFF)**

Receive VLAN Data Table (0 and 1)

This table is used for data to support receive VLAN tagging, VLAN stripping, and VLAN translation. The table is always 4K entries deep but the width depends on how many of the VLAN functions are included at build time. VLAN translation requires 12 bits at each location while VLAN stripping and VLAN tagging require 1 bit each at each location.

When all receive VLAN functions are included, the table is 14 bits wide. If VLAN functions are not included, the bits for those functions will not be present and writes to those bits will have no effect while reads will return zero.

The table may be either 1-bit, 2-bits, 12-bits, 13-bits, or 14-bits wide depending on which features are present. The table must be initialized by software via the PLB and is addressed on 32-bit word boundaries.

The receive VLAN Table entry with all VLAN functions present is shown in Figure 22 while Figure 23 shows the receive VLAN Table entry with only the translation field. Note that the bit locations for the functions do not change even when some functions are not used in the build.

Please see the section on VLAN functions for more details ("Extended VLAN Support" on page 93).

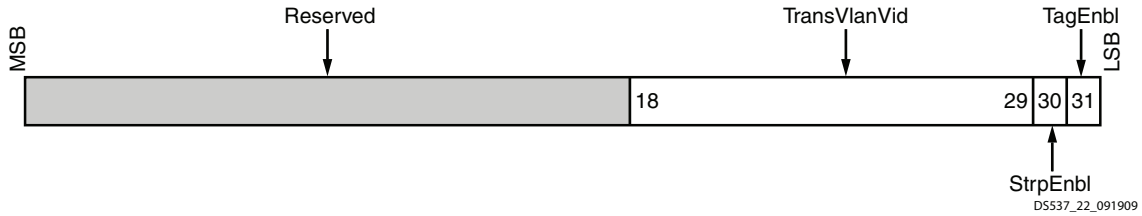

Figure 22: **Receive VLAN Table entry w/ all fields (offset 0x8000-0xBFFF and 0x48000-0x4BFFF)**

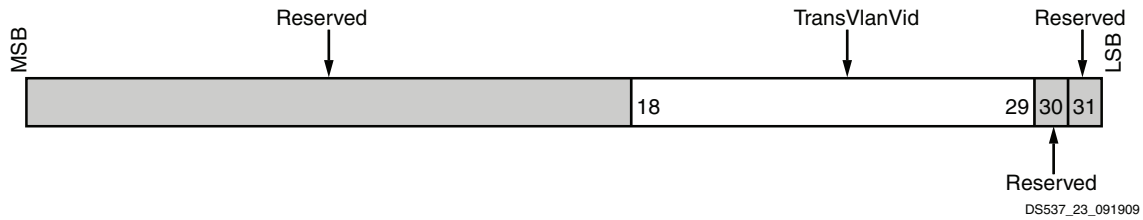

Figure 23: **Receive VLAN Table entry w/ one field (offset 0x8000-0xBFFF and 0x48000-0x4BFFF)**

Statistics Counters (0 and 1)

The set of 64-bit counters are only present when selected at build-time. The counters keep track of statistics for the transmit and receive Ethernet traffic and are defined in Table 22.

Table 22: **Statistics Counter locations**

Offset (TEMAC0/TEMAC1)	Name	Description
0x200 / 0x40200	Transmitted bytes (lower 32 bits)	(TXBL0, TXBL1) A count of bytes of frames transmitted (destination address to frame check sequence inclusive).
0x204 / 0x40204	Transmitted bytes (upper 32 bits)	(TXBU0, TXBU0) A count of bytes of frames transmitted (destination address to frame check sequence inclusive).
0x208 / 0x40208	Received bytes (lower 32 bits)	(RXBL0, RXBL1) A count of bytes of frames received (destination address to frame check sequence inclusive).
0x20C / 0x4020C	Received bytes (upper 32 bits)	(RXBU0, RXBU1) A count of bytes of frames received (destination address to frame check sequence inclusive).
0x210 / 0x40210	Undersize frames received (lower 32 bits)	(RXUNDRL0, RXUNDRL1) A count of the number of frames received (less than 64 bytes in length) but otherwise well formed.
0x214 / 0x40214	Undersize frames received (upper 32 bits)	(RXUNDRU0, RXUNDRU1) A count of the number of frames received (less than 64 bytes in length) but otherwise well formed.
0x218 / 0x40218	Fragment frames received (lower 32 bits)	(RXFRAGL0, RXFRAGL1) A count of the number of frames received (less than 64 bytes in length) with a bad frame check sequence field.
0x21C / 0x4021C	Fragment frames received (upper 32 bits)	(RXFRAGU0, RXFRAGU1) A count of the number of frames received (less than 64 bytes in length) with a bad frame check sequence field.
0x220 / 0x40220	64 byte Frames Received OK (lower 32 bits)	(RX64BL0, RX64BL1) A count of error-free frames received that were 64 bytes in length.
0x224 / 0x40224	64 byte Frames Received OK (upper 32 bits)	(RX64BU0, RX64BU1) A count of error-free frames received that were 64 bytes in length.
0x228 / 0x40228	65-127 byte Frames Received OK (lower 32 bits)	(RX65B127L0, RX65B127L1) A count of error-free frames received that were between 65 and 127 bytes in length.
0x22C / 0x4022C	65-127 byte Frames Received OK (upper 32 bits)	(RX65B127U0, RX65B127U1) A count of error-free frames received that were between 65 and 127 bytes in length.
0x230 / 0x40230	128-255 byte Frames Received OK (lower 32 bits)	(RX128B255L0, RX128B255L1) A count of error-free frames received that were between 128 and 255 bytes in length.
0x234 / 0x40234	128-255 byte Frames Received OK (upper 32 bits)	(RX128B255U0, RX128B255U1) A count of error-free frames received that were between 128 and 255 bytes in length.
0x238 / 0x40238	256-511 byte Frames Received OK (lower 32 bits)	(RX256B511L0, RX256B511L1) A count of error-free frames received that were between 256 and 511 bytes in length.

Table 22: **Statistics Counter locations *(Cont'd)***

Offset (TEMAC0/TEMAC1)	Name	Description
0x23C / 0x4023C	256-511 byte Frames Received OK (upper 32 bits)	(RX256B511U0, RX256B511U1) A count of error-free frames received that were between 256 and 511 bytes in length.
0x240 / 0x40240	512-1023 byte Frames Received OK (lower 32 bits)	(RX512B1023L0, RX512B1023L1) A count of error-free frames received that were between 512 and 1023 bytes in length.
0x244 / 0x40244	512-1023 byte Frames Received OK (upper 32 bits)	(RX512B1023U0), (RX512B1023U1) A count of error-free frames received that were between 512 and 1023 bytes in length.
0x248 / 0x40248	1024-MaxFrameSize byte Frames Received OK (lower 32 bits)	(RX1024BL0, RX1024BL1) A count of error-free frames received that were between 1024 bytes and the specified IEEE 802.3-2002 maximum legal length.
0x24C / 0x4024C	1024-MaxFrameSize byte Frames Received OK (upper 32 bits)	(RX1024BU0, RX1024BU1) A count of error-free frames received that were between 1024 bytes and the specified IEEE 802.3-2002 maximum legal length.
0x250 / 0x40250	Oversize Frames Received OK (lower 32 bits)	(RXOVRL0, RXOVRL1) A count of otherwise error-free frames received that exceeded the maximum legal frame length specified in IEEE 802.3-2002.
0x254 / 0x40254	Oversize Frames Received OK (upper 32 bits)	(RXOVRU0, RXOVRU1) A count of otherwise error-free frames received that exceeded the maximum legal frame length specified in IEEE 802.3-2002.
0x258 / 0x40258	64 byte Frames Transmitted OK (lower 32 bits)	(TX64BL0, TX64BL1) A count of error-free frames transmitted that were 64 bytes in length.
0x25C / 0x4025C	64 byte Frames Transmitted OK (upper 32 bits)	(TX64BU0, TX64BU1) A count of error-free frames transmitted that were 64 bytes in length.
0x260 / 0x40260	65-127 byte Frames Transmitted OK (lower 32 bits)	(TX65B127L0, TX65B127L1) A count of error-free frames transmitted that were between 65 and 127 bytes in length.
0x264 / 0x40264	65-127 byte Frames Transmitted OK (upper 32 bits)	(TX65B127U0, TX65B127U1) A count of error-free frames transmitted that were between 65 and 127 bytes in length.
0x268 / 0x40268	128-255 byte Frames Transmitted OK (lower 32 bits)	(TX128B255L0, TX128B255L1) A count of error-free frames transmitted that were between 128 and 255 bytes in length.
0x26C / 0x4026C	128-255 byte Frames Transmitted OK (upper 32 bits)	(TX128B255U0, TX128B255U1) A count of error-free frames transmitted that were between 128 and 255 bytes in length.
0x270 / 0x40270	256-511 byte Frames Transmitted OK (lower 32 bits)	(TX256B511L0, TX256B511L1) A count of error-free frames transmitted that were between 256 and 511 bytes in length.
0x274 / 0x40274	256-511 byte Frames Transmitted OK (upper 32 bits)	(TX256B511U0, TX256B511U1) A count of error-free frames transmitted that were between 256 and 511 bytes in length.

Table 22: **Statistics Counter locations *(Cont'd)***

Offset (TEMAC0/TEMAC1)	Name	Description
0x278 / 0x40278	512-1023 byte Frames Transmitted OK (lower 32 bits)	(TX512B1023L0, TX512B1023L1) A count of error-free frames transmitted that were between 512 and 1023 bytes in length.
0x27C / 0x4027C	512-1023 byte Frames Transmitted OK (upper 32 bits)	(TX512B1023U0, TX512B1023U1) A count of error-free frames transmitted that were between 512 and 1023 bytes in length.
0x280 / 0x40280	1024-MaxFrameSize byte Frames Transmitted OK (lower 32 bits)	(TX1024BL0, TX1024BL1) A count of error-free frames transmitted that were between 1024 and the specified IEEE 802.3-2002 maximum legal length.
0x284 / 0x40284	1024-MaxFrameSize byte Frames Transmitted OK (upper 32 bits)	TX1025BU0, TX1025BU1) A count of error-free frames transmitted that were between 1024 and the specified IEEE 802.3-2002 maximum legal length.
0x288 / 0x40288	Oversize Frames Transmitted OK (lower 32 bits)	(TXOVRL0, TXOVRL1) A count of otherwise error-free frames transmitted that exceeded the maximum legal frame length specified in IEEE 802.3-2002.
0x28C / 0x4028C	Oversize Frames Transmitted OK (upper 32 bits)	(TXOVRU0, TXOVRU1) A count of otherwise error-free frames transmitted that exceeded the maximum legal frame length specified in IEEE 802.3-2002.
0x290 / 0x40290	Frames Received OK (lower 32 bits)	(RXFL0, RXFL1) A count of error-free frames received.
0x294 / 0x40294	Frames Received OK (upper 32 bits)	(RXFU0, RXFU1) A count of error-free frames received.
0x298 / 0x40298	Frame Check Sequence Errors (lower 32 bits)	(RXFCSERL0, RXFCSERL1) A count of received frames that failed the CRC check and were at least 64 bytes in length.
0x29C / 0x4029C	Frame Check Sequence Errors (upper 32 bits)	(RXFCSERU0, RXFCSERU1) A count of received frames that failed the CRC check and were at least 64 bytes in length.
0x2A0 / 0x402A0	Broadcast Frames Received OK (lower 32 bits)	(RXBCSTFL0, RXBCSTFL1) A count of frames that were successfully received and were directed to the broadcast group address.
0x2A4 / 0x402A4	Broadcast Frames Received OK (upper 32 bits)	(RXBCSTFU0, RXBCSTFU1) A count of frames that were successfully received and were directed to the broadcast group address.
0x2A8 / 0x402A8	Multicast Frames Received OK (lower 32 bits)	(RXMCSTFL0, RXMCSTFL1) A count of frames that were successfully received and were directed to a non broadcast group address.
0x2AC / 0x402AC	Multicast Frames Received OK (upper 32 bits)	(RXMCSTFU0, RXMCSTFU1) A count of frames that were successfully received and were directed to a non broadcast group address.
0x2B0 / 0x402B0	Control Frames Received OK (lower 32 bits)	(RXCTRFL0, RXCTRFL1) A count of error-free frames received that contained the special Control Frame identifier in the length/type field.
0x2B4 / 0x402B4	Control Frames Received OK (upper 32 bits)	(RXCTRFU0, RXCTRFU1) A count of error-free frames received that contained the special Control Frame identifier in the length/type field.

Table 22: **Statistics Counter locations *(Cont'd)***

Offset (TEMAC0/TEMAC1)	Name	Description
0x2B8 / 0x402B8	Length/Type Out of Range (lower 32 bits)	(RXLTERL0, RXLTERL1) A count of frames received that were at least 64 bytes in length where the length/type field contained a length value that did not match the number of MAC client data bytes received. The counter also increments for frames in which the length/type field indicated that the frame contained padding, but where the number of MAC client data bytes received was greater than 64 bytes (minimum frame size). The exception to the this is when the Length/Type Error Checks are disabled in the chosen MAC, which case this counter will not increment.
0x2BC / 0x402BC	Length/Type Out of Range (upper 32 bits)	(RXLTERU0, RXLTERU1) A count of frames received that were at least 64 bytes in length where the length/type field contained a length value that did not match the number of MAC client data bytes received. The counter also increments for frames in which the length/type field indicated that the frame contained padding, but where the number of MAC client data bytes received was greater than 64 bytes (minimum frame size). The exception to the this is when the Length/Type Error Checks are disabled in the chosen MAC, which case this counter will not increment.
0x2C0 / 0x402C0	VLAN Tagged Frames Received OK (lower 32 bits)	(RXVLANFL0, RXVLANFL1) A count of error-free VLAN frames received. This counter will only increment when the receiver is configured for VLAN operation
0x2C4 / 0x402C4	VLAN Tagged Frames Received OK (upper 32 bits)	RXVLANFU0, RXVLANFU1) A count of error-free VLAN frames received. This counter will only increment when the receiver is configured for VLAN operation
0x2C8 / 0x402C8	Pause Frames Received OK (lower 32 bits)	(RXPFL0, RXPFL1) A count of error-free frames received that: Contained the MAC Control type identifier 88-08 in the length/type field Contained a destination address that matched either the MAC Control multicast address or the configured source address of the MAC Contained the PAUSE opcode Were acted upon by the MAC
0x2CC / 0x402CC	Pause Frames Received OK (upper 32 bits)	(RXPFU0, RXPFU1) A count of error-free frames received that: Contained the MAC Control type identifier 88-08 in the length/type field Contained a destination address that matched either the MAC Control multicast address or the configured source address of the MAC Contained the PAUSE opcode Were acted upon by the MAC
0x2D0 / 0x402D0	Control Frames Received with Unsupported Opcode (lower 32 bits)	(RXUOPFL0, RXUOPFL1) A count of error-free frames received that contained the MAC Control type identifier 88-08 in the length/type field but were received with an opcode other than the PAUSE opcode.

Table 22: **Statistics Counter locations *(Cont'd)***

Offset (TEMAC0/TEMAC1)	Name	Description
0x2D4 / 0x402D4	Control Frames Received with Unsupported Opcode (upper 32 bits)	(RXUOPFU0, RXUOPFU1) A count of error-free frames received that contained the MAC Control type identifier 88-08 in the length/type field but were received with an opcode other than the PAUSE opcode.
0x2D8 / 0x402D8	Frames Transmitted OK (lower 32 bits)	(TXFL0, TXFL1) A count of error-free frames transmitted.
0x2DC / 0x402DC	Frames Transmitted OK (upper 32 bits)	(TXFU0, TXFU1) A count of error-free frames transmitted.
0x2E0 / 0x402E0	Broadcast Frames Transmitted OK (lower 32 bits)	(TXBCSTFL0, TXBCSTFL1) A count of error-free frames that were transmitted to the broadcast address.
0x2E4 / 0x402E4	Broadcast Frames Transmitted OK (upper 32 bits)	(TXBCSTFU0, TXBCSTFU1) A count of error-free frames that were transmitted to the broadcast address.
0x2E8 / 0x402E8	Multicast Frames Transmitted OK (lower 32 bits)	(TXMCSTFL0, TXMCSTFL1) A count of error-free frames that were transmitted to a group destination address other than broadcast.
0x2EC / 0x402EC	Multicast Frames Transmitted OK (upper 32 bits)	(TXMCSTFU0, TXMCSTFU1) A count of error-free frames that were transmitted to a group destination address other than broadcast.
0x2F0 / 0x402F0	Underrun Errors (lower 32 bits)	(TXUNDRERL0, TXUNDRERL1) A count of frames that would otherwise be transmitted by the core but could not be completed due to the assertion of TX_UNDERRUN during the frame transmission.
0x2F4 / 0x402F4	Underrun Errors (upper 32 bits)	(TXUNDRERU0, TXUNDRERU1) A count of frames that would otherwise be transmitted by the core but could not be completed due to the assertion of TX_UNDERRUN during the frame transmission.
0x2F8 / 0x402F8	Control Frames Transmitted OK (lower 32 bits)	(TXCTRFL0, TXCTRFL1) A count of error-free frames transmitted that contained the MAC Control Frame type identifier 88-08 in the length/type field.
0x2FC / 0x402FC	Control Frames Transmitted OK (upper 32 bits)	(TXCTRFU0, TXCTRFU1) A count of error-free frames transmitted that contained the MAC Control Frame type identifier 88-08 in the length/type field.
0x300 / 0x40300	VLAN Tagged Frames Transmitted OK (lower 32 bits)	(TXVLANFL0, TXVLANFL1) A count of error-free VLAN frames transmitted. This counter will only increment when the transmitter is configured for VLAN operation.
0x304 / 0x40304	VLAN Tagged Frames Transmitted OK (upper 32 bits)	(TXVLANFU0, TXVLANFU1) A count of error-free VLAN frames transmitted. This counter will only increment when the transmitter is configured for VLAN operation.
0x308 / 0x40308	Pause Frames Transmitted OK (lower 32 bits)	(TXPFL0, TXPFL1) A count of error-free PAUSE frames generated and transmitted by the MAC in response to an assertion of pause_req.
0x30C / 0x4030C	Pause Frames Transmitted OK (upper 32 bits)	(TXPFU0, TXPFU1) A count of error-free PAUSE frames generated and transmitted by the MAC in response to an assertion of pause_req.

Directly Addressable TEMAC Registers

TEMAC Most Significant Word Data (shared) Register (MSW)

The Most Significant Data Word Register is shown in Figure 24. This register is used when reading from the Multicast Address table. For all other transactions only the LSW register is used. This register is shared between the Ethernet Interface 0 and Ethernet Interface 1 so data for one interface can be overwritten by data for the other interface even though each interface has its own address for this register.

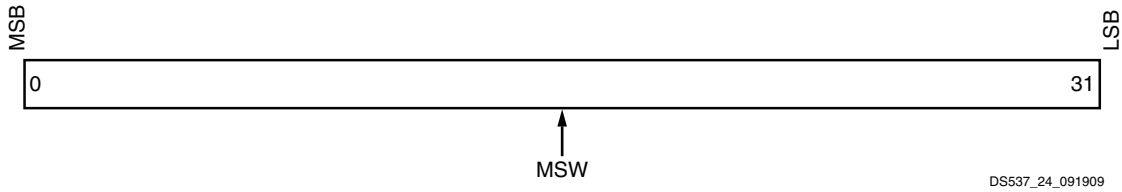

Figure 24: **TEMAC Most Significant Word Data Register (offset 0x020 or 0x060)**

Table 23 shows the TEMAC Most Significant Word Data Register bit definitions.

Table 23: **TEMAC Most Significant Word Data Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 31	MSW	Read/Write	undefined	**Most Significant Data Word.** Data from the Multicast Address table or fabric registers to the PLB for read operations.

TEMAC Least Significant Word Data (shared) Register (LSW)

The Least Significant Data Word Register is shown in Figure 25. This register is used when writing or reading all of the indirectly addressable registers. This register is shared between the Ethernet Interface 0 and Ethernet Interface 1 so data for one interface can be overwritten by data for the other interface even though each interface has its own address for this register.

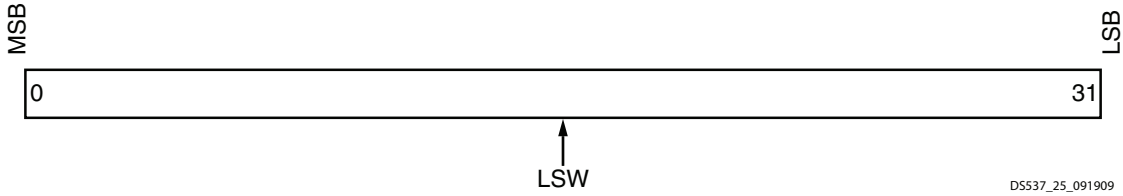

Figure 25: **TEMAC Least Significant Word Data Register (offset 0x024 or 0x064)**

Table 24 shows the TEMAC Least Significant Word Data Register bit definitions.

Table 24: **TEMAC Least Significant Word Data Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 31	LSW	Read/Write	undefined	**Least Significant Data Word.** Data input from the PLB data bus for writes to the indirectly addressable registers or data from the indirectly addressable registers to the PLB for read operations.

TEMAC Control (shared) Register (CTL)

The Control Register is shown in Figure 26. Writing to this register initiates a write to or read from the indirectly addressable registers. If it is a write operation, the LSW must be provided with the write value prior to writing to this register. This register is shared between the Ethernet Interface 0 and Ethernet Interface 1 even though each interface has its own address for this register.

It is important to note that once an access has been initiated to an indirectly addressed location, the interface will ignore any additional requests for indirect register accesses until the current access is complete. Therefore, it is essential to determine that the current access is complete before issuing a new indirect access command. While some indirect accesses will complete in one clock cycle, others such as accessing PHY registers from the MII Management interface will require many clock cycles.

Determining that an indirect access is complete can be accomplished with two methods using either polling or interrupts.

1. An interrupt indicates that the access is complete. The interrupt HardAcsCmplt must be enabled in the TIE register as well as the IE register. The interrupt must be cleared as described later in this document in the section discussing the interrupt registers.
2. Polling the ready status register (RDY) to determine if the access is complete. The bits in this register are asserted when there is no access in progress. When an access is in progress, a bit corresponding to the type of access is de-asserted. When the access is complete, the bit is re-asserted.

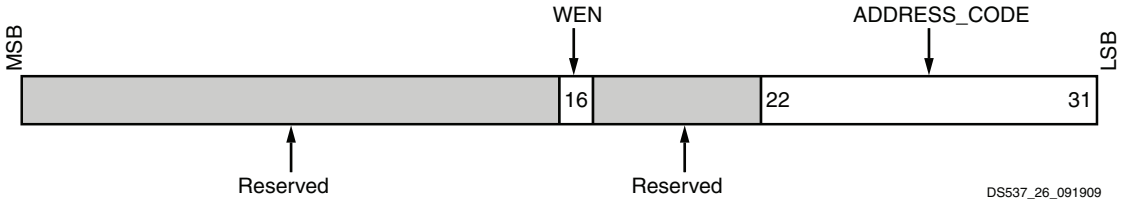

Figure 26: **TEMAC Control Register (offset 0x028 or 0x068)**

Table 25 shows the TEMAC Control Register bit definitions.

Table 25: **TEMAC Control Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
22 - 31	ADDRESS_CODE	Read/Write	0x0	**Address Code.** The address in this field selects the indirectly addressable register that will be access with a read or a write as shown in Table 8 and Figure 4.
17 - 21	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.
16	WEN	Read/Write	0	**Write Enable.** When this bit is asserted, the data in the LSW register is written to the register indicated by the ADDRESS_CODE field. 0 - read operation 1 - write operation
0 - 15	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

TEMAC Ready Status Register Ethernet Interface 0 (RDY0)

The Ready Status Register is shown in Figure 27. This register is read only. The bits in the RDY register are asserted when there is no access in progress. When an access is in progress, a bit corresponding to the type of access is automatically de-asserted. The bit is automatically re-asserted when the access is complete.

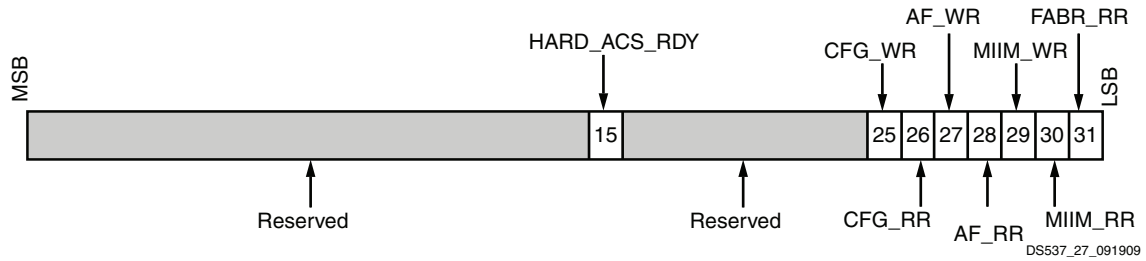

Figure 27: **TEMAC Ready Status Register Ethernet Interface 0 (offset 0x02C)**

Table 26 shows the TEMAC Ready Status Register Ethernet Interface 0 bit definitions.

Table 26: **TEMAC Ready Status Register Ethernet Interface 0 Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	FABR_RR	Read	1	**Fabric Read Ready Interface 0.** This bit is set (ready) when no fabric based registers read operation is pending. Includes ADDRESS_CODE values of 0x000 - 0x02F and 0x040 - 0x04F. These address ranges are not currently supported. 0 - a fabric register read operation is in progress 1 - all pending fabric read operations are complete
30	MIIM_RR	Read	1	**MII Management Read Ready Interface 0.** This bit is set (ready) when no MII Management registers read operation is pending. Corresponds to ADDRESS_CODE 0x3B4. 0 - a MIIM register read operation is in progress 1 - all pending MIIM read operations are complete
29	MIIM_WR	Read	1	**MII Management Write Ready Interface 0.** This bit is set (ready) when no MII Management registers write operation is pending. Corresponds to ADDRESS_CODE 0x3B4. 0 - a MIIM register write operation is in progress 1 - all pending MIIM write operations are complete
28	AF_RR	Read	1	**Address Filter Read Ready Interface 0.** This bit is set (ready) when no address filter registers write operation is pending. Includes ADDRESS_CODE values of 0x380 - 0x390. 0 - a address filter register write operation is in progress 1 - all pending address filter write operations are complete
27	AF_WR	Read	1	**Address Filter Write Ready Interface 0.** This bit is set (ready) when no address filter registers write operation is pending. Includes ADDRESS_CODE values of 0x380 - 0x390. 0 - a address filter register write operation is in progress 1 - all pending address filter write operations are complete

Table 26: **TEMAC Ready Status Register Ethernet Interface 0 Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
26	CFG_RR	Read	1	**Configuration Register Read Ready Interface 0.** This bit is set (ready) when no configuration registers write operation is pending. Includes ADDRESS_CODE values of 0x200 - 0x340. 0 - a configuration register write operation is in progress 1 - all pending configuration write operations are complete
25	CFG_WR	Read	1	**Configuration Register Write Ready Interface 0.** This bit is set (ready) when no configuration registers write operation is pending. Includes ADDRESS_CODE values of 0x200 - 0x340. 0 - a configuration register write operation is in progress 1 - all pending configuration write operations are complete
16 - 24	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.
15	HARD_ACS _RDY	Read	1	**Hard register Access Ready Interface 0.** This bit is set (ready) when all other used bits in this Ready Status register are set. 0 - an access operation is in progress 1 - all pending access operations are complete
0 - 14	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

TEMAC Ready Status Register Ethernet Interface 1 (RDY1)

The Ready Status Register is shown in Figure 28. This register is read only. The bits in the RDY register are asserted when there is no access in progress. When an access is in progress, a bit corresponding to the type of access is automatically de-asserted. The bit is automatically re-asserted when the access is complete.

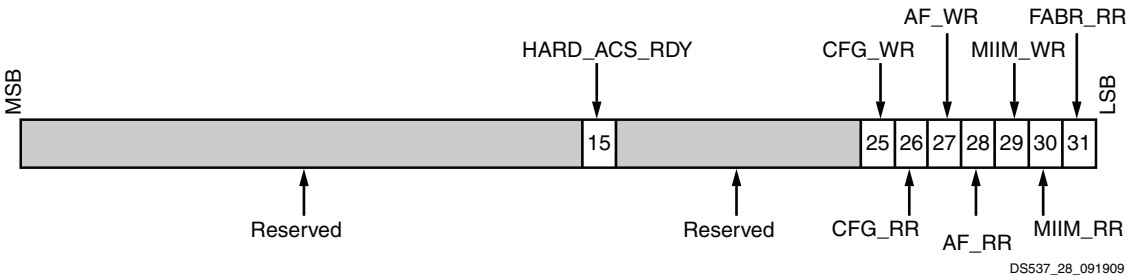

Figure 28: **Hard TEMAC Ready Status Register Ethernet Interface 1 (offset 0x06C)**

Table 27 shows the TEMAC Ready Status Register Ethernet Interface 1 bit definitions.

Table 27: **TEMAC Ready Status Register Ethernet Interface 1 Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	FABR_RR	Read	1	**Fabric Read Ready Interface 1.** This bit is set (ready) when no fabric based registers read operation is pending. Includes ADDRESS_CODE values of 0x000 - 0x02F and 0x040 - 0x04F. These address ranges are not currently supported. 0 - a fabric register read operation is in progress 1 - all pending fabric read operations are complete
30	MIIM_RR	Read	1	**MII Management Read Ready Interface 1.** This bit is set (ready) when no MII Management registers read operation is pending. Corresponds to ADDRESS_CODE 0x3B4. 0 - a MIIM register read operation is in progress 1 - all pending MIIM read operations are complete
29	MIIM_WR	Read	1	**MII Management Write Ready Interface 1.** This bit is set (ready) when no MII Management registers write operation is pending. Corresponds to ADDRESS_CODE 0x3B4. 0 - a MIIM register write operation is in progress 1 - all pending MIIM write operations are complete
28	AF_RR	Read	1	**Address Filter Read Ready Interface 1.** This bit is set (ready) when no address filter registers write operation is pending. Includes ADDRESS_CODE values of 0x380 - 0x390. 0 - a address filter register write operation is in progress 1 - all pending address filter write operations are complete
27	AF_WR	Read	1	**Address Filter Write Ready Interface 1.** This bit is set (ready) when no address filter registers write operation is pending. Includes ADDRESS_CODE values of 0x380 - 0x390. 0 - a address filter register write operation is in progress 1 - all pending address filter write operations are complete
26	CFG_RR	Read	1	**Configuration Register Read Ready Interface 1.** This bit is set (ready) when no configuration registers write operation is pending. Includes ADDRESS_CODE values of 0x200 - 0x340. 0 - a configuration register write operation is in progress 1 - all pending configuration write operations are complete
25	CFG_WR	Read	1	**Configuration Register Write Ready Interface 1.** This bit is set (ready) when no configuration registers write operation is pending. Includes ADDRESS_CODE values of 0x200 - 0x340. 0 - a configuration register write operation is in progress 1 - all pending configuration write operations are complete
16 - 24	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.
15	HARD_ACS _RDY	Read	1	**Hard register Access Ready Interface 1.** This bit is set (ready) when all other used bits in this Ready Status register are set. 0 - an access operation is in progress 1 - all pending access operations are complete
0 - 14	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

Indirectly Addressable TEMAC Registers

TEMAC Receive Configuration Word 0 (RCW0) Registers

The TEMAC Receive Configuration Word 0 Register is shown in Figure 29. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers. These registers can be written at any time but the receiver logic will only apply the configuration changes during Inter Frame gaps.

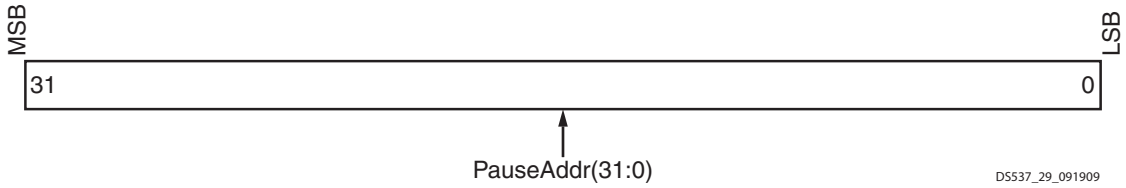

Figure 29: **EMAC Receive Configuration Word 0 (RCW0) Registers (ADDRESS_CODE 0x200)**

Table 28 shows the TEMAC Receive Configuration Word 0 Registers bit definitions.

Table 28: **TEMAC Receive Configuration Word 0 (RCW0) Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	PauseAddr	Read/Write	0xDDC CBBAA	**Pause Frame Ethernet MAC Address (31:0).** This address is used to match the destination address of any received flow control frames. It is also used as the source address for any transmitted flow control frames. This address is ordered so that the first byte transmitted/ received is the lowest position byte in the register. For example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in the PauseAddr(47:0) as 0xFFEED-DCCBBAA.

TEMAC Receive Configuration Word 1 (RCW1) Registers

The TEMAC Receive Configuration Word 1 Register is shown in Figure 30. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers. These registers can be written at any time but the receiver logic will only apply the configuration changes during Inter Frame gaps. The exception to this is the Reset bit which is effective immediately.

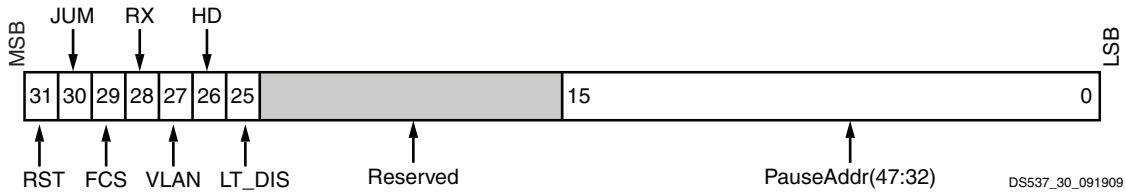

Figure 30: **TEMAC Receive Configuration Word 1 (RCW1) Registers (ADDRESS_CODE 0x240)**

Table 29 shows the TEMAC Receive Configuration Word1 Registers bit definitions.

Table 29: **TEMAC Receive Configuration Word1 (RCW1) Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	RST	Read/Write	0	**Reset.** When this bit is "1", the receiver is reset. The bit automatically resets to "0". The reset also sets all of the receiver configuration registers to their default values. 0 - no reset 1 - initiate a receiver reset
30	JUM1(1)	Read/Write	1	**Jumbo Frame Enable.** When this bit is "1" the receiver accepts frames over the maximum length specified in IEEE Std 802.3-2002 specification. 0 - receive jumbo frames disabled 1 - receive jumbo frames enabled
29	FCS	Read/Write	1	**In-Band FCS Enable.** When this bit is "1", the receiver provides the FCS field with the rest of the frame data. When this bit is "0" the FCS field is stripped from the receive frame data. In either case the FCS field is verified. 0 - strip the FCS field from the receive frame data 1 - provide the FCS field with the receive frame data
28	RX	Read/Write	1	**Receive Enable.** When this bit is "1", the receiver logic is enabled to operate. When this bit is "0", the receiver ignores activity on the receive interface. 0 - receive disabled 1 - receive enabled
27	VLAN(2)	Read/Write	1	**VLAN Frame Enable.** When this bit is "1", the receiver accepts VLAN tagged frames. The maximum payload length increases by four bytes. 0 - receive of VLAN frames disabled 1 - receive of VLAN frames enabled
26	HD	Read/Write	0	**Half-Duplex Mode.** When this bit is "1", the receive operates in half-duplex mode. When this bit is "0", the receiver operates in full-duplex mode. Only full-duplex is supported so this bit should always be set to "0". 0 - full-duplex receive 1 - half-duplex receive (not supported)
25	LT_DIS	Read/Write	0	**Length/Type Field Valid Check Disable.** When this bit is "1", it disables the Length/Type field check on the receive frame. 0 - perform Length/Type field check 1 - do not perform Length/Type field check
24 - 16	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

Table 29: **TEMAC Receive Configuration Word1 (RCW1) Registers Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
15 - 0	PauseAddr	Read/Write	0xFFEE	**Pause Frame Ethernet MAC Address (47:32).** This address is used to match the destination address of any received flow control frames. It is also used as the source address for any transmitted flow control frames. This address is ordered so that the first byte transmitted/ received is the lowest position byte in the register. For example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in the PauseAddr(47:0) as 0xFFEEDDCCBBAA.

1. Extended VLAN function require that jumbo frames be enabled (1).
2. This bit enables basic VLAN operation that is native to the TEMAC core. The TEMAC core recognizes VLAN frames when the Type/Length field contains a VLAN TAG with a TPID value of 0x8100. No other TPID values are recognized. Extended VLAN mode described later allow programmable TPID values. This bit must be '0' (disabled) when using extended VLAN mode.

TEMAC Transmit Configuration (TC) Registers

The TEMAC Transmit Configuration Register is shown in Figure 31. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers. These registers can be written at any time but the transmitter logic will only apply the configuration changes during Inter Frame gaps. The exception to this is the Reset bit which is effective immediately.

Figure 31: **TEMAC Transmit Configuration Registers (ADDRESS_CODE 0x280)**

Table 30 shows the TEMAC Transmit Configuration Registers bit definitions.

Table 30: **TEMAC Transmit Configuration Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	RST	Read/Write	0	**Reset.** When this bit is "1", the transmitter is reset. The bit automatically resets to "0". The reset also sets all of the transmitter configuration registers to their default values. 0 - no reset 1 - initiate a transmitter reset
30	JUM(1)	Read/Write	1	**Jumbo Frame Enable.** When this bit is "1" the transmitter sends frames over the maximum length specified in IEEE Std 802.3-2002 specification. 0 - send jumbo frames disabled 1 - send jumbo frames enabled

Table 30: **TEMAC Transmit Configuration Registers Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
29	FCS	Read/Write	0	**In-Band FCS Enable.** When this bit is "1", the transmitter accepts the FCS field with the rest of the frame data. When this bit is "0" the FCS field is calculated and supplied by the transmitter. In either case the FCS field is verified. 0 - transmitter calculates and sends FCS field 1 - FCS field is provided with transmit frame data
28	TX	Read/Write	1	**Transmit Enable.** When this bit is "1", the transmit logic is enabled to operate. 0 - transmit disabled 1 - transmit enabled
27	VLAN(2)	Read/Write	1	**VLAN Frame Enable.** When this bit is "1", the transmitter allows transmission of VLAN tagged frames. 0 - transmit of VLAN frames disabled 1 - transmit of VLAN frames enabled
26	HD	Read/Write	0	**Half-Duplex Mode.** When this bit is "1", the transmitter operates in half-duplex mode. When this bit is "0", the transmitter operates in full-duplex mode. Only full-duplex is supported so this bit should always be set to "0". 0 - full-duplex receive 1 - half-duplex receive (not supported)
25	IFG	Read/Write	1	**Inter Frame Gap Adjustment Enable.** When this bit is "1", the transmitter uses the value of the IFGP register (Figure 7) to extend the transmit Inter Frame Gap beyond the minimum of 12 idle cycles (96-bit times on the Ethernet Interface). 0 - no IFGP adjustment enabled 1 - IFGP adjusted based on IFGP register
0 - 24	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

1. Extended VLAN function require that jumbo frames be enabled (1).
2. This bit enables basic VLAN operation that is native to the TEMAC core. The TEMAC core recognizes VLAN frames when the Type/Length field contains a VLAN TAG with a TPID value of 0x8100. No other TPID values are recognized. Extended VLAN mode described later allow programmable TPID values. This bit must be '0' (disabled) when using extended VLAN mode.

TEMAC Flow Control Configuration (FCC) Registers

The TEMAC Flow Control Configuration Register is shown in Figure 32. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers. These registers can be written at any time but the flow control logic will only apply the configuration changes during Inter Frame gaps.

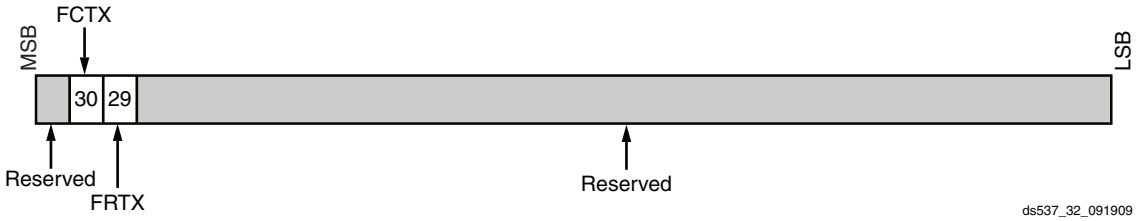

Figure 32: **TEMAC Flow Control Configuration Registers (ADDRESS_CODE 0x2C0)**

Table 31 shows the TEMAC Flow Control Configuration Registers bit definitions.

Table 31: **TEMAC Flow Control Configuration Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	Reserved	Read	0	**Reserved.** These bits are reserved for future definition and will always return zero.
30	FCTX	Read/Write	1	**Transmit Flow Control Enable.** When this bit is “1”, the transmitter will send a flow control frame when a value is written to the TPF register (page 31). 0 - transmit flow control frame disabled 1 - transmit flow control frame enabled
29	FCRX	Read/Write	1	**Receive Flow Control Enable.** When this bit is "1", the receive flow control frames inhibit transmitter operation. When this bit is "0", the flow control frames are passed through with other receive frames. 0 - receive flow control disabled 1 - receive flow control enabled
0 - 20	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

TEMAC Ethernet MAC Mode Configuration (EMMC) Registers

The TEMAC Ethernet MAC Mode Configuration Register is shown in Figure 33. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface’s register is accessed is controlled by the address used to access the LSW and CTL registers. These registers can be written at any time but the Ethernet interface will only apply the configuration changes during Inter Frame gaps. This register is slightly different for implementations using the soft TEMAC (C_TEMAC_TYPE = 2), Virtex-4 hard TEMAC (C_TEMAC_TYPE = 1), Virtex-5 hard TEMAC (C_TEMAC_TYPE = 0), and Virtex-6 hard TEMAC (C_TEMAC_TYPE = 3).

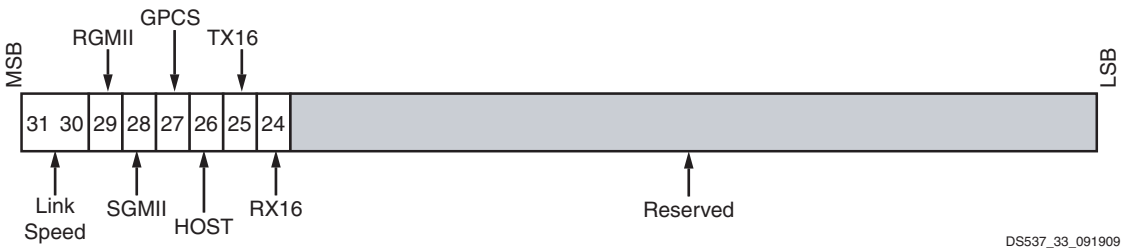

Figure 33: **TEMAC Ethernet MAC Mode Configuration Registers (ADDRESS_CODE 0x300)**

Table 32 shows the TEMAC Ethernet MAC Mode Configuration Registers bit definitions.

Table 32: **TEMAC Ethernet MAC Mode Configuration Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31 - 30	Link Speed	Read/Write(1)	10 / 01(2)	**Link Speed Selection.** The speed of the Ethernet interface is defined by the following values. 10 - 1000 Mb/S 01 - 100 Mb/S 00 - 10 Mb/s 11 - N/A
29	RGMII	Read Read/Write(1)	0	**RGMII Mode Enable.** When this bit is "1", the Ethernet interface is configured in RGMII mode. 0 - not configured in RGMII mode 1 - configured in RGMII mode
28	SGMII	Read Read/Write(1)	0	**SGMII Mode Enable.** When this bit is "1", the Ethernet interface is configured in SGMII mode. 0 - not configured in SGMII mode 1 - configured in SGMII mode
27	GPCS	Read Read/Write(1)	0	**1000BASE-X Mode Enable.** When this bit is "1", the Ethernet interface is configured in 1000BASE-X mode. 0 - not configured in 1000BASE-X mode 1 - configured in 1000BASE-X mode
26	HOST	Read Read/Write(1)	1 / 0(3)	**Host Interface Enable.** When this bit is "1", the host interface is enabled. 0 - host interface disabled 1 - host interface is enabled
25	TX16	Read Read/Write(1)	0	**Transmit 16-bit Data Interface Enable.** When this bit is "1" and 1000BASE-X is being used, the transmit data interface is 16-bits wide. When this bit is "0", the transmit data interface is 8-bits wide. The 16-bit interface is not supported so this bit should always return "0". 0 - 8-bit transmit data interface 1 - 16-bit transmit data interface
24	RX16	Read Read/Write(1)	0	**Receive 16-bit Data Interface Enable.** When this bit is "1" and 1000BASE-X is being used, the receive data interface is 16-bits wide. When this bit is "0", the receive data interface is 8-bits wide. The 16-bit interface is not supported so this bit should always return "0". 0 - 8-bit receive data interface 1 - 16-bit receive data interface
0 - 20	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

1. The entire contents of this register are Read/Write accessible for the Virtex-6 hard TEMAC configuration, but only bits 31-30 are Read/Write accessible in Virtex-4, Virtex-5, and Soft TEMAC configurations
2. The Reset Value for LINK SPEED is “10” or 1000 Mb/s for all PHY interfaces except for MII which is not capable of that speed. The Reset Value for LINK SPEED for the MII interface is “01” or 100 Mb/s.
3. The use or not of the Host interface is hidden from the user and is of no concern. However, this register will return a different reset value for different TEMAC implementations. The soft TEMAC implementation will return a ’0’ while the Virtex-4 hard TEMAC, Virtex-5 hard TEMAC, and Virtex-6 hard TEMAC implementations will return a ’1’.

TEMAC RGMII/SGMII Configuration (PHYC) Registers

The TEMAC RGMII/SGMII Configuration Register is shown in Figure 34. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers.

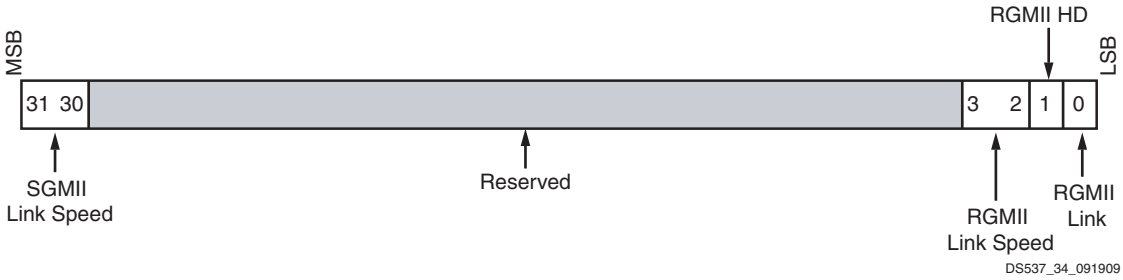

Figure 34: **TEMAC RGMII/SGMII Configuration Registers (ADDRESS_CODE 0x320)**

Table 33 shows the TEMAC RGMII/SGMII Configuration Registers bit definitions.

Table 33: **TEMAC RGMII/SGMII Configuration Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31 - 30	SGMII Link Speed	Read	0x0	**SGMII Link Speed.** Valid in SGMII mode only. This displays the SGMII speed information as received from auto negotiation by the speed field of the PCS/PMA register 5 (Table 105).The speed of the Ethernet interface is defined by the following values. 10 - 1000 Mb/S 01 - 100 Mb/S 00 - 10 Mb/s 11 - N/A
4 - 29	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.
2 - 3	RGMII Link Speed	Read	0x0	**RGMII Link Speed.** Valid in RGMII mode only. This displays the RGMII speed information as encoded by the PHY to the TEMAC by GMII_RX_DV and GMII_RX_ER during the IFG. The speed of the Ethernet interface is defined by the following values. 10 - 1000 Mb/S 01 - 100 Mb/S 00 - 10 Mb/s 11 - N/A
1	RGMII HD	Read	0	**RGMII Half-Duplex Mode.** Valid in RGMII mode only. When this bit is "1", the interface operates in half-duplex mode. When this bit is "0", the interface operates in full-duplex mode. This information is encoded by the PHY to the TEMAC by GMII_RX_DV and GMII_RX_ER during the IFG. 0 - full-duplex 1 - half-duplex
0	RGMII Link	Read	0	**RGMII Link.** Valid in RGMII mode only. When this bit is "1", the is up. When this bit is "0", the link is down. This information is encoded by the PHY to the TEMAC by GMII_RX_DV and GMII_RX_ER during the IFG. 0 - link is down 1 - link is up

TEMAC Management Configuration (MC) Registers

The TEMAC Management Configuration Register is shown in Figure 35. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers.

This register provides control for the TEMAC PHY MII management (MDIO) interface. The MDIO interface supplies a clock to the external devices, MDC_0 and MDC_1. This clock is derived from the HostClk input signal using the value in the Clock Divide[5:0].

The frequency of the MDIO clock is given by the following equation:

$$f_{MDC} = \frac{f_{HOSTCLK}}{(1 + \text{Clock Divide}[5:0]) \times 2}$$

To comply with the IEEE 802.3-2002 specification for this interface, the frequency of MDC_0 and MDC_1 should not exceed 2.5 MHz.

To prevent MDC_0 and MDC_1 from being out of specification, the Clock Divide[5:0] value powers up at 000000. While this value is in the register, it is impossible to enable the MDIO interface.

Even if the MDIO interface is enabled by setting bit 25 of this register, the MDIO port will still be disabled until a non-zero value has been written into the clock divide field.

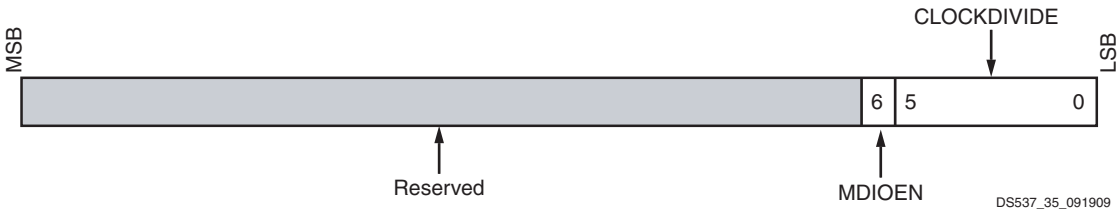

Figure 35: **TEMAC Management Configuration Registers (ADDRESS_CODE 0x340)**

Table 34 shows the TEMAC Management Configuration Registers bit definitions.

Table 34: **TEMAC Management Configuration Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
7 - 31	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.
6	MDIOEN	Read/Write	0	**MDIO Enable.** When this bit is "1", the MDIO (MII Management) interface is used to access the PHY. 0 - MDIO disabled 1 - MDIO enabled
0 - 5	CLOCK DIVIDE	Read/Write	0x0	**Clock Divide.** This value is used to derive the MDC (MII Management interface clock) signal. The maximum permitted frequency is 2.5 MHz.

TEMAC Unicast Address Word 0 (UAW0) Registers

The TEMAC Unicast Address Word 0 Register is shown in Figure 36. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers.

The Unicast Addresses Registers combine to provide a 48 bit ethernet station address. Word 0 provides the low order 32 bits of the address while word 1 provides the high order 16 bits.

This register's reset value is slightly different for implementations using the soft TEMAC (C_TEMAC_TYPE = 2), Virtex-4 hard TEMAC (C_TEMAC_TYPE = 1), Virtex-5 hard TEMAC (C_TEMAC_TYPE = 0), and Virtex-6 hard TEMAC (C_TEMAC_TYPE = 3).

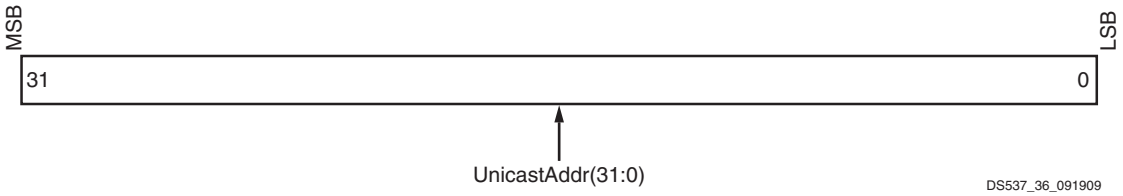

Figure 36: **TEMAC Unicast Address Word 0 Registers (ADDRESS_CODE 0x380)**

Table 35 shows the TEMAC Unicast Address Word 0 Registers bit definitions.

Table 35: **TEMAC Unicast Address Word 0 Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 31	UnicastAddr	Read/Write	0xDDCCBBAA 0xFFFFFFFF(1)	**Unicast Address (31:0).** This address is used to match against the destination address of any received frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA.

1. This register will return a different reset value for different TEMAC implementations. The soft TEMAC implementation will return a 0xFFFFFFFF while the Virtex-4 hard TEMAC, Virtex-5 hard TEMAC and Virtex-6 hard TEMAC implementations will return a 0xDDCCBBAA.

TEMAC Unicast Address Word 1 (UAW1) Registers

The TEMAC Unicast Address Word 1 Register is shown in Figure 37. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers.

The Unicast Addresses Registers combine to provide a 48 bit ethernet station address. Word 0 provides the low order 32 bits of the address while word 1 provides the high order 16 bits.

This register's reset value is slightly different for implementations using the soft TEMAC (C_TEMAC_TYPE = 2), Virtex-4 hard TEMAC (C_TEMAC_TYPE = 1), Virtex-5 hard TEMAC (C_TEMAC_TYPE = 0), and Virtex-6 hard TEMAC (C_TEMAC_TYPE = 3).

Figure 37: **TEMAC Unicast Address Word 1 Registers (ADDRESS_CODE 0x384)**

Table 36 shows the TEMAC Unicast Address Word 1 Registers bit definitions.

Table 36: **TEMAC Unicast Address Word 1 Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
16 - 31	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.
0 - 15	UnicastAddr	Read/Write	0x0000FFEE 0xFFFFFFFF (1)	**Unicast Address (47:32).** This address is used to match against the destination address of any received frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA.

1. This register will return a different reset value for different TEMAC implementations. The soft TEMAC implementation will return a 0xFFFFFFFF while the Virtex-4 hard TEMAC, Virtex-5 hard TEMAC and Virtex-6 hard TEMAC implementations will return a 0x0000FFEE.

TEMAC Multicast Address Table Access Word 0 (MAW0) Registers

The TEMAC Multicast Address Table Access Word 0 Register is shown in Figure 38. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers.

The Multicast Addresses Table Access Word 0 and Word 1 registers combine to provide a 48 bit ethernet addresses to store in Multicast Address Table which can hold up to 4 addresses. (Filtering of more than 4 multicast addresses can be achieved by including the extended multicast address function at build-time.) These two registers also provide a place to store addresses being read from the Multicast Address Table.

Word 0 provides the low order 32 bits of the address while word 1 provides the high order 16 bits. Word 1 also provides the table entry address and the read or write control signal. Figure 39 shows how word 0 and word 1 registers combine to make a Multicast Address Table entry.

The reset values stored in the 4 Multicast Address Table entries is slightly different for implementations using the soft TEMAC (C_TEMAC_TYPE = 2), Virtex-4 hard TEMAC (C_TEMAC_TYPE = 1), Virtex-5 hard TEMAC (C_TEMAC_TYPE = 0), and Virtex-6 hard TEMAC (C_TEMAC_TYPE = 3). After reset, a soft TEMAC implementation will return 0xFFFFFFFF for all multicast address table entries while Virtex-4 hard TEMAC, Virtex-5 hard TEMAC and Virtex-6 hard TEMAC implementations will return 0x00000000 for all multicast address table entries.

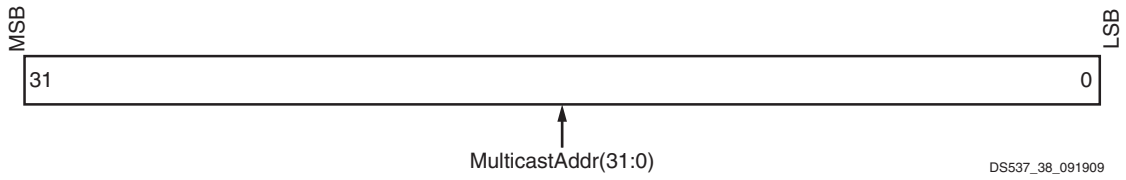

Figure 38: **TEMAC Multicast Address Table Access Word 0 Registers (ADDRESS_CODE 0x388)**

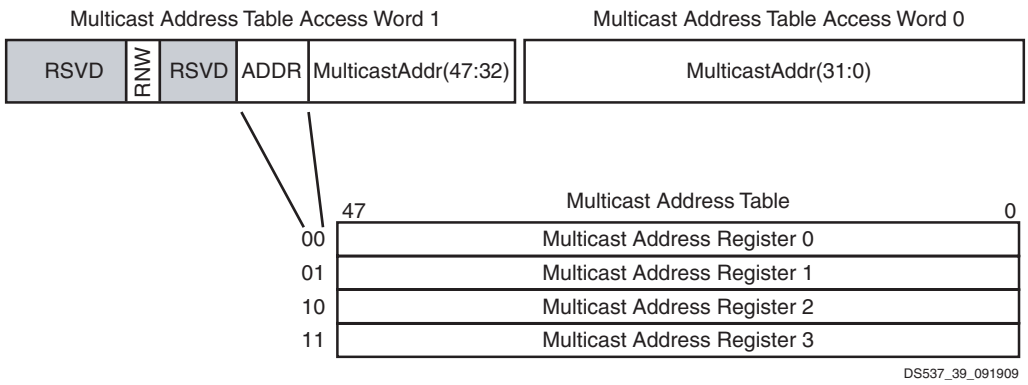

Figure 39: **Multicast Address Table Diagram**

Table 37 shows the TEMAC Multicast Address Table Access Word 0 Registers bit definitions.

Table 37: **TEMAC Multicast Address Table Access Word 0 Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 31	MulticastAddr	Read/Write	0x0	**Multicast Address (31:0).** The multicast address bits are temporarily deposited into this register for writing into a multicast address table register. When a read from a multicast address table register has been performed, the multicast address bits will be accessible from this register. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA.

TEMAC Multicast Address Table Access Word 1 (MAW1) Registers

The TEMAC Multicast Address Table Access Word 1 Register is shown in Figure 40. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers.

The Multicast Addresses Table Access Word 0 and Word 1 registers combine to provide a 48 bit ethernet addresses to store in Multicast Address Table which can hold up to 4 addresses. These two registers also provide a place to store addresses being read from the Multicast Address Table.

Word 0 provides the low order 32 bits of the address while word 1 provides the high order 16 bits. Word 1 also provides the table entry address and the read or write control signal. Figure 39 shows how word 0 and word 1 registers combine to make a Multicast Address Table entry.

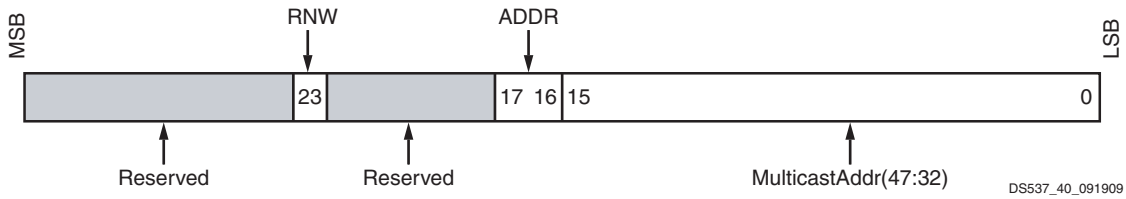

Figure 40: **TEMAC Multicast Address Table Access Word 1 Registers (ADDRESS_CODE 0x38C)**

Table 38 shows the TEMAC Multicast Address Table Access Word 1 Registers bit definitions.

Table 38: **TEMAC Multicast Address Table Access Word 1 Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
24 - 31	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.
23	RNW	Read/Write	0	**Multicast Address Table Register Read Enable.** When this bit is "1", a multicast address table register is read. When this bit is "0", a multicast address table register is written. 0 - write operation 1 - read operation
18 - 22	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.
16 - 17	ADDR	Read/Write	0x0	**Multicast Address Table Register Address.** This value is used to choose the multicast address table register to access. 00 - multicast address table register 0 01 - multicast address table register 1 10 - multicast address table register 2 11 - multicast address table register 3
0 - 15	MulticastAddr	Read/Write	0x0	**Multicast Address (47:32).** The multicast address bits are temporarily deposited into this register for writing into a multicast address table register. When a read from a multicast address table register has been performed, the multicast address bits will be accessible from this register. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA.

Writing to the Multicast Address Table Registers

For writing to the desired multicast address table register, two write operations must be performed as follows:

1. Write to the LSW register (using the Ethernet interface 0 address or the Ethernet interface 1 address as appropriate) with the value for the Multicast Address Table Access Word 0 [the multicast address (31:0) value].
2. Write to the CTL register (using the same Ethernet interface as in step 1) setting the write enable (WEN) bit and providing ADDRESS_CODE 0x388. This is initiates a write to the Multicast Address Table Access Word 0 register.
3. Poll the RDY register for the Ethernet interface being accessed until the AF_WR bit is asserted or wait until the HardAcsCmplt interrupt is asserted.
4. Write to the LSW register (again using the same Ethernet interface) with the value for the Multicast Address Table Access Word 1 [the multicast address (47:32) value, Write Enable bit set to 0, and the 2-bit address of the Multicast Address Table register to be written].
5. Write to the CTL register (using the same Ethernet interface) setting the write enable (WEN) bit and providing ADDRESS_CODE 0x38C. This is initiates a write to the Multicast Address Table Access Word 1 register. Writing to the Multicast Address Table Access Word 1 initiates the update of the selected register (one of four possible) in the Multicast Address Table.

6. Poll the RDY register for the Ethernet interface being accessed until the AF_WR bit is asserted or wait until the HardAcsCmplt interrupt is asserted.

Table 39: **Example of a Write to a Multicast Address Table Register**

Register	Access	Value	Activity
LSW0	Write	0xDDCCBBAA	Write the lower part of the multicast address that will go to the Multicast Address Table Access Word 0 register for Ethernet interface 0
CTL0	Write	0x00008388	Initiate the write to the Multicast Address Table Access Word 0 register by setting the write enable and providing the address for that indirectly addressed register
RDY0	Read	0x0001007F or 0x0000006F	Poll ready register for Ethernet interface 0 until we see 0x0001007F indicating that the Address Filter register write access is complete
LSW0	Write	0x0002FFEE	Write the upper part of the multicast address that will go to the Multicast Address Table Access Word 1 register for Ethernet interface 0 along with the address of the Multicast Address Table register we will write (2 in this case) and set the write enable bit to 0
CTL0	Write	0x0000838C	Initiate the write to the Multicast Address Table Access Word 1 register by setting the write enable and providing the address for that indirectly addressed register
RDY0	Read	0x0001007F or 0x0000006F	Poll ready register for Ethernet interface 0 until we see 0x0001007F indicating that the Address Filter register write access is complete

Reading from the Multicast Address Table Registers

To read the desired multicast address table register, a PLB write must be performed as follows:

1. Write to the LSW register (using the Ethernet interface 0 address or the Ethernet interface 1 address as appropriate) with the value for the Multicast Address Table Access Word 1 [the Write Enable bit set to 1 and the 2-bit address of the Multicast Address Table register to be written].
2. Write to the CTL register (using the same Ethernet interface) setting the write enable (WEN) bit and providing ADDRESS_CODE 0x38C. This is initiates a write to the Multicast Address Table Access Word 1 register.
3. Poll the RDY register for the Ethernet interface being accessed until the AF_RR bit is asserted or wait until the HardAcsCmplt interrupt is asserted.
4. Read the MSW and LSW (using the same Ethernet interface) to return the multicast address (47:32) and multicast address (31:0) respectively for the Multicast Address Table Register selected.

Table 40: **Example of a Read from a Multicast Address Table Register**

Register	Access	Value	Activity
LSW1	Write	0x00830000	Write the information that will go into the Multicast Address Table Access Word 1 register for Ethernet interface 1 including the address of the Multicast Address Table register we will read (3 in this case) and set the write enable bit to 1
CTL1	Write	0x0000838C	Initiate the write to the Multicast Address Table Access Word 1 register by setting the write enable and providing the address for that indirectly addressed register

Table 40: **Example of a Read from a Multicast Address Table Register**

Register	Access	Value	Activity
RDY1	Read	0x0001007F or 0x00000077	Poll ready register for Ethernet interface 1 until we see 0x0001007F indicating that the Address Filter register read access is complete
LSW1	Read	data word	Read the lower part of the multicast address that is in the Multicast Address Table register we read
MSW1	Read	data word	Read the upper part of the multicast address that is in the Multicast Address Table register we read

TEMAC Address Filter Mode (AFM) Registers

The TEMAC Address Filter Mode Register is shown in Figure 41. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers.

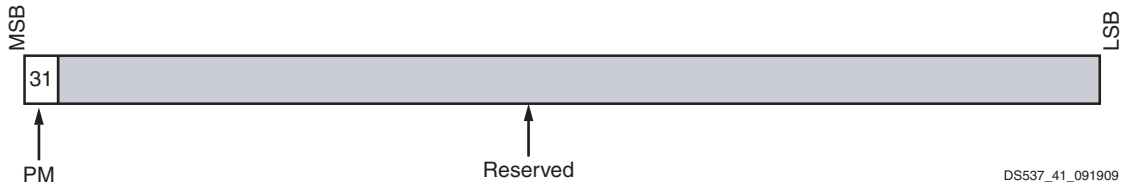

Figure 41: **TEMAC Address Filter Mode Registers (ADDRESS_CODE 0x390)**

Table 41 shows the TEMAC Address Filter Mode Registers bit definitions.

Table 41: **TEMAC Address Filter Mode Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	PM(1)	Read/Write	0	**Promiscuous Receive Address Mode Enable.** When this bit is "1", the receive address filtering is disabled and all destination addresses are accepted. When this bit "0", the receive address filtering is enabled. 0 - address filtering enabled 1 - address filtering disabled (all addresses accepted)
0 - 30	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

1. Extended Multicast Filtering require the promiscuous mode be enabled/ address filtering is disabled (1)

TEMAC Interrupt Status (TIS) Registers

The TEMAC Interrupt Status register is shown in Figure 42. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers.

The TEMAC Interrupt Status registers and Interrupt Enable registers are used as part of the overall XPS_LL_TEMAC interrupt control (Figure 9).

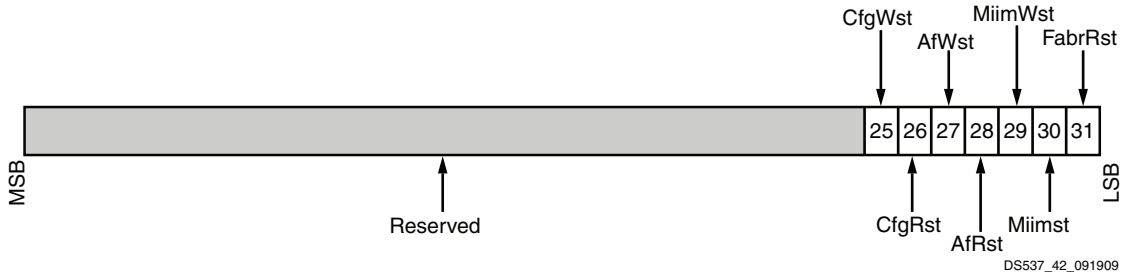

Figure 42: **TEMAC Interrupt Status Registers (ADDRESS_CODE 0x3A0)**

Table 42 shows the TEMAC Interrupt Status Registers bit definitions.

Table 42: **TEMAC Interrupt Status Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	FABR RST	Read/Write	0	**Fabric Read Interrupt Status.** This bit indicates that a read access of a fabric register has completed. 0 - no interrupt pending 1 - interrupt pending
30	MIIM RST	Read/Write	0	**MII Management Read Interrupt Status.** This bit indicates that a read access of a register using the MII management interface has completed. 0 - no interrupt pending 1 - interrupt pending
29	MIIM WST	Read/Write	0	**MII Management Write Interrupt Status.** This bit indicates that a write access of a register using the MII management interface has completed. 0 - no interrupt pending 1 - interrupt pending
28	AF RST	Read/Write	0	**Address Filter Read Interrupt Status.** This bit indicates that a read access of a multicast address table register has completed. 0 - no interrupt pending 1 - interrupt pending
27	AF WST	Read/Write	0	**Address Filter Write Interrupt Status.** This bit indicates that a write access of a multicast address table register has completed. 0 - no interrupt pending 1 - interrupt pending
26	CFG RST	Read/Write	0	**Configuration Read Interrupt Status.** This bit indicates that a read access of a configuration register has completed. 0 - no interrupt pending 1 - interrupt pending
25	CFG WST	Read/Write	0	**Configuration Write Interrupt Status.** This bit indicates that a write access of a configuration register has completed. 0 - no interrupt pending 1 - interrupt pending
0 - 24	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

Table 43: **Example of a Read and Clear of the TEMAC Interrupt Status Register**

Register	Access	Value	Activity
CTL0	Write	0x000003A0	Initiate the read from the Interrupt Status register by clearing the write enable and providing the address for that indirectly addressed register
LSW0	Read	data word	Read the current Interrupt Status register value
LSW0	Write	0x00000000	Write all zeros in preparation for transferring it to the Interrupt Status register thus clearing all interrupts
CTL0	Write	0x000083A0	Initiate the write to the Interrupt Status register by setting the write enable and providing the address for that indirectly addressed register

TEMAC Interrupt Enable (TIE) Registers

The TEMAC Interrupt Enable Register is shown in Figure 43. There is a separate register for each of the two Ethernet Interfaces. Determination of which Ethernet Interface's register is accessed is controlled by the address used to access the LSW and CTL registers.

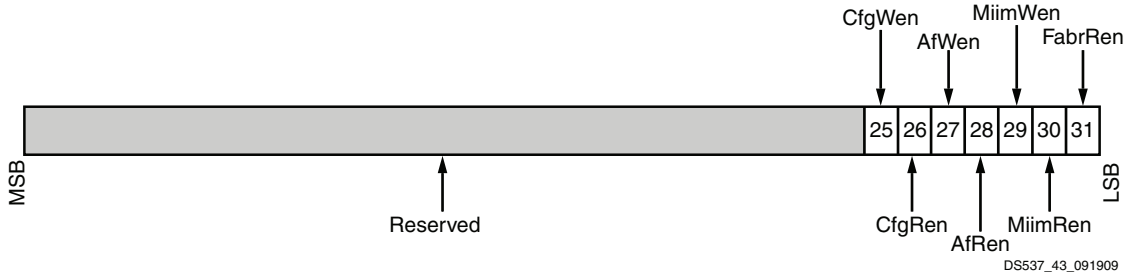

Figure 43: **TEMAC Interrupt Enable Registers (ADDRESS_CODE 0x3A4)**

Table 44 shows the TEMAC Interrupt Enable Registers bit definitions.

Table 44: **TEMAC Interrupt Enable Registers Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31	FABR REN	Read/Write	0	**Fabric Read Interrupt Enable.** This bit enables a completion interrupt for a read access of a fabric register. 0 - no interrupt enabled 1 - interrupt enabled
30	MIIM REN	Read/Write	0	**MII Management Read Interrupt Enable.** This bit enables completion interrupt for a read access of a register using the MII management interface. 0 - no interrupt enabled 1 - interrupt enabled
29	MIIM WEN	Read/Write	0	**MII Management Write Interrupt Enable.** This bit enables completion interrupt for a write access of a register using the MII management interface. 0 - no interrupt enabled 1 - interrupt enabled

Table 44: **TEMAC Interrupt Enable Registers Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
28	AF REN	Read/Write	0	**Address Filter Read Interrupt Enable.** This bit enables completion interrupt for a read access of a multicast address table register. 0 - no interrupt enabled 1 - interrupt enabled
27	AF WEN	Read/Write	0	**Address Filter Write Interrupt Enable.** This bit enables completion interrupt for a write access of a multicast address table register. 0 - no interrupt enabled 1 - interrupt enabled
26	CFG REN	Read/Write	0	**Configuration Read Interrupt Enable.** This bit enables completion interrupt for a read access of a configuration register. 0 - no interrupt enabled 1 - interrupt enabled
25	CFG WEN	Read/Write	0	**Configuration Write Interrupt Enable.** This bit enables completion interrupt for a write access of a configuration register. 0 - no interrupt enabled 1 - interrupt enabled
0 - 24	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

Table 45 shows an examples of a Read and Set of the TEMAC Interrupt Enable Register.

Table 45: **Example of a Read and Set of the TEMAC Interrupt Enable Register**

Register	Access	Value	Activity
CTL0	Write	0x000003A4	Initiate the read from the Interrupt Enable register by clearing the write enable and providing the address for that indirectly addressed register
LSW0	Read	data word	Read the current Interrupt Enable register value
LSW0	Write	0x0000007F	Write all ones in preparation for transferring it to the Interrupt Enable register thus enabling all interrupts
CTL0	Write	0x000083A4	Initiate the write to the Interrupt Enable register by setting the write enable and providing the address for that indirectly addressed register

TEMAC MII Management Write Data (MIIMWD) Register

The TEMAC MII Management Write Data Register is shown in Figure 44. This register is shared between the two Ethernet interfaces and is a temporary storage location for data to be written to a PHY register (internal or external) via the MII Management interface. Only one register is needed for the two Ethernet interfaces because a PLB access of a MII Management register can not be initiated until the previous access is complete (and, as a result, the register is available for use). The MII Management write is initiated by writing to the MII Management Access Initiate Register address after providing the data to this register and the PHY address and register address to the LSW register.

This register is only used for writing to PHY registers. When reading from PHY registers, the data will be stored in the LSW register. For more information on using the MII Management interface for access-

ing PHY registers, please See "Using the MII Management to Access Internal or External PHY Registers" on page 73.

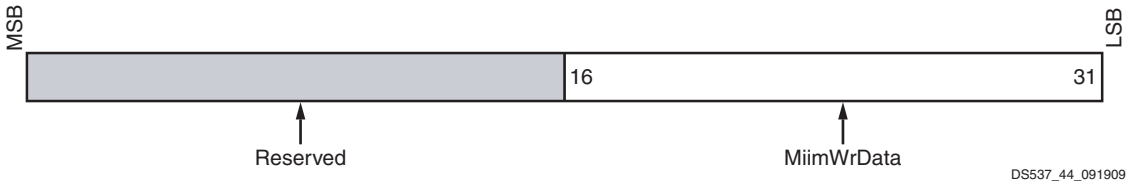

Figure 44: **TEMAC MII Management Write Data Register (ADDRESS_CODE 0x3B0)**

Table 46 shows the TEMAC MII Management Write Data Register bit definitions.

Table 46: **TEMAC MII Management Write Data Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
16 - 31	MiimWrData	Read/Write	0x0	**MII Management Write Data.** This field temporarily holds data to be written to a PHY register.
0 - 15	Reserved	Read	0x0	**Reserved.** These bits are reserved for future definition and will always return zero.

TEMAC MII Management Access Initiate (MIIMAI) Register

The TEMAC MII Management Access Initiate Register is not actually a register at all. A write to this address location initiates a MII Management write or read access to a PHY register either internal or external to the XPS_LL_TEMAC. No data is actually stored at this address.

During a write operation the data in the LSW register is used to address the PHY and the PHY register. The MII Management Write Data register holds the data that is written to the PHY register. During a read operation the LSW register is used to address the PHY and the PHY register and the data from the PHY register is stored back in the LSW register.

Using the MII Management to Access Internal or External PHY Registers

The MII Management interface is used to access PHY registers either in devices external to the FPGA or, in the case of SGMII or 1000BASE-X PHYs, PHY registers internal to the Hard TEMAC silicon component as described in "Internal 1000BASE-X PCS/PMA Management Registers" on page 119 and "Internal SGMII Management Registers" on page 125.

Prior to any MII Management accesses taking place, the Management Configuration register must be written with a valid CLOCK_DIVIDE value and the MDIOEN bit must be set.

The determination as to which PHYs registers are accessed is by the value of the PHY_ADDR field. Each PHY, internal or external, should have a unique 5-bit PHY address excluding "00000" which is define as a broadcast PHY address.

The MII Management interface is defined in IEEE Std 802.3, Clause 22 as a two-wire interface with a shared bi-directional serial data bus and a clock with a maximum permitted frequency of 2.5 MHz. As a result, MII Management access can take many PLB clock cycles to complete.

To write to a PHY register, the data must be written to the MII Management Data register. The PHY address and register number are written to the LSW register. Writing to the MII Management Access

Initiate register address starts the operation. The format of the PHYAD and REGAD in the LSW register is shown in Figure 45.

To read from a PHY register, the PHY address and register number are written to the LSW register. Writing to the MII Management Access Initiate register address starts the operation. When the operation completes, the PHY register value is available in the LSW register.

To access the internal SGMII or 1000BASE-X registers, the PHYAD should match that set by parameters C_TEMAC0_PHYADDR or C_TEMAC1_PHYADDR.

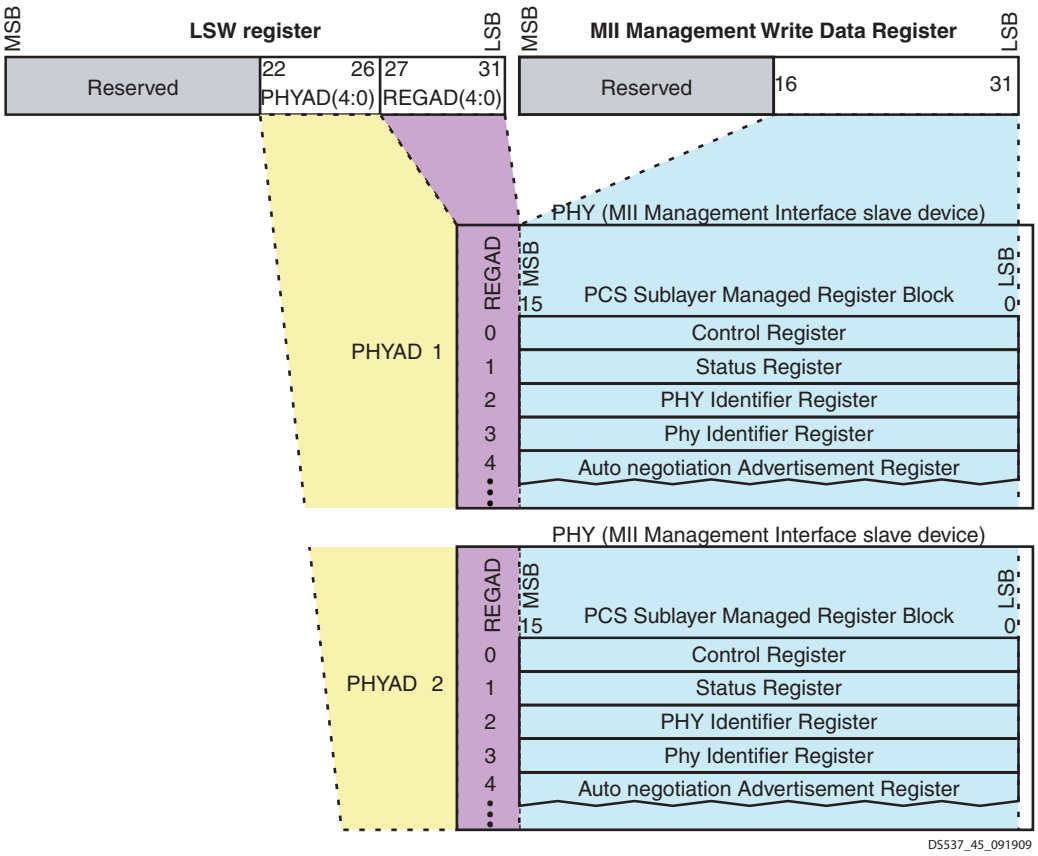

Figure 45: **MII Management Write Register Field Mapping**

Table 47 provides an example of a PHY register Write via the MII Management Interface.

Table 47: **Example of a PHY Register Write via the MII Management Interface**

Register	Access	Value	Activity
LSW0	Write	0x0000ABCD	Write the value that will be written to the PHY register (we chose 0xABCD for this case).
CTL0	Write	0x000083B0	Initiate the write to the MII Management Data register by setting the write enable and providing the address for that indirectly addressed register.

Table 47: **Example of a PHY Register Write via the MII Management Interface**

Register	Access	Value	Activity
LSW0	Write	0x00000062	Write the PHYAD (3 in this case) and REGAD (2 in this case) to the LSW register for Ethernet interface 0.
CTL0	Write	0x000083B4	Initiate the write to the MII Management Access Initiate register by setting the write enable and providing the address for that indirectly addressed register. This will start the transaction on the MII Management Interface to the PHY.
RDY0	Read	0x0001007F or 0x0000007B	Poll ready register for Ethernet interface 0 until we see 0x0001007F indicating that the MII Management Interface write access is complete.

Table 48: **Example of a PHY Register Read via the MII Management Interface**

Register	Access	Value	Activity
LSW1	Write	0x000000AF	Write the PHYAD (5 in this case) and REGAD (15 in this case) to the LSW register for Ethernet interface 1.
CTL1	Write	0x000003B4	Initiate the read from the MII Management Access Initiate register by clearing the write enable and providing the address for that indirectly addressed register. This will start the transaction on the MII Management Interface to the PHY.
RDY1	Read	0x0001007F or 0x0000007D	Poll ready register for Ethernet interface 1 until we see 0x0001007F indicating that the MII Management Interface write access is complete.
LSW1	Read	data word	Read the data value received from the PHY register.

Including or Excluding I/O in the Physical Interfaces

In order to allow the XPS_LL_TEMAC to be easy to use, the core includes BUFG, IBUFG, IBUF, OBUF and other FPGA resources to correctly connect the external interface signals to the FPGA I/O.

Some users may find that this prevents them from being able to make custom connections on these signals which may be required for their system. By setting the parameter C_INCLUDE_IO to “0”, these resources will not be automatically provided. In this case the user will be responsible for making the appropriate connections.

TCP/UDP Checksum Off Load in Hardware

When using TCP or UDP Ethernet protocols, data integrity is maintained by calculating and verifying checksum values over the TCP and UDP frame data. Normally this checksum functionality is handled by the protocol stack software which can be relatively slow and use significant processor utilization for large frames at high Ethernet data rates.

An alternative is to off load some of this transmit checksum generation and receive checksum verification in hardware. This is possible by including checksum off loading in the XPS_LL_TEMAC using parameters. Including the checksum off load functions are a trade off between using more FPGA resources and getting higher Ethernet performance while freeing up processor use for other functions.

When using the TCP/UDP checksum off load function, checksum information is passed between the software and the XPS_LL_TEMAC by using the header and footer fields in the transmit and receive

LocalLink data interface frames. Table 49, Table 50, Table 51, and Table 55 show the checksum off load fields.

The use of the TCP / UPD checksum off load function requires that the core connected to the XPS_LL_TEMAC via the LocalLink also supports the LocalLink header and footer fields. While any custom core may be created to source and sink data on the LocalLink, the cores provided by Xilinx at the time of the writing of this data sheet include the XPS_LL_FIFO_V1_02_A (which does not support these LocalLink fields), the SDMA_v2_00_B which is part of the MPMC_V5_04_A and the Hard DMA included in the PowerPC 440 Processor block (both of which do support these LocalLink fields). Please refer to the Mapping Xilinx DMA Buffer Descriptor Fields to LocalLink Fields section for more information.

TX_CSBEGIN is the beginning offset which points to the first byte that needs to be included in the checksum calculation. The first byte is indicated by a value of zero. The beginning position must be 16 bit aligned. With TCP and UDP you would want to set this value to skip over the Ethernet frame header as well as the IP datagram header so that the checksumming is started in the proper place in the TCP or UDP segment. Operating systems may provide functions to calculate this value as it is normally variable based on the variable IP datagram header size. In all cases, the TX_CSBEGIN value must be 14 or larger to be valid.

TX_CSINSERT is the offset which points to the location where the checksum value should be written into the TCP or UDP segment header. This value must be 16 bit aligned and can not be in the first 8 bytes of the frame. Again, operating systems may provide functions to calculate this value as it is normally variable based on the variable IP datagram header size.

TX_CSCNTRL is a 16 bit field however only the least significant bit is defined. This bit will control the insertion of the checksum into the frame data. If set to a "1" then the checksum will be written into the transmit frame otherwise not modification of the frame will occur.

TX_CSINIT is a 16-bit seed that can be used to insert the TCP or UDP pseudo header into the checksum calculation. In many cases the protocol stack will calculate the pseudo header checksum value and place it in the header checksum field of the transmit frame. In those cases this field should be zeroed. If the protocol stack does not provide the pseudo header checksum in the header checksum field location of the transmit frame, then that field should be zeroed and the pseudo header checksum value must be calculated and placed in the TX_CSINIT field of the buffer descriptor.

In order for the transmit checksum to be calculated correctly, the transmit Ethernet FCS must not be provided as part of the transmit data and the transmit FCS calculation and insertion must be enabled in the XPS_LL_TEMAC.

There is a special case for checksums of UDP datagrams. From the UDP RFC 768:

> If the computed checksum is zero, it is transmitted as all ones (the equivalent in one's complement arithmetic). An all zero transmitted checksum value means that the transmitter generated no checksum (for debugging or for higher level protocols that don't care).

If the frame encapsulates a UDP datagram, and if the resulting checksum is zero, then a value of all ones is used. This case does not exist for TCP because a checksum of zero is legal.

RX_CSRAW is the raw receive checksum calculated over the entire Ethernet payload. It is calculated starting at byte 14 of the Ethernet frame (the byte following the Type/Length field) and continues until the end of the Ethernet frame. If the receive Ethernet FCS stripping is not enabled in the XPS_LL_TEMAC, the FCS will also be included in the checksum. The application is required to calculate the checksum of the fields which should not have been included to subtract them from the RAW

checksum value. In most cases, the protocol software which allows receive checksum off loading will require a pass or fail indication. The application will have to compare the adjusted raw checksum value with the checksum field of the TCP or UDP header and provide the pass or fail indication.

LocalLink Transmit and Receive Data Interfaces

The Ethernet frame data to be transmitted and the frame data that is received passes between the XPS_LL_TEMAC and the rest of the embedded system via Xilinx LocalLink interfaces. In many cases the other end of the LocalLink interfaces will be connected to a DMA controller that in some devices is Hard IP located in silicon and in other devices is soft IP implemented in FPGA fabric.

However, any custom logic may be used to connect to the LocalLink interface as long as it meets the requirements of the XPS_LL_TEMAC LocalLink interface.

The LocalLink interface is a high-performance, synchronous, point-to-point connection which, in its general use case, is described in its specification listed in the Referenced Documents (page 155).

This section will describe the specific 32-bit implementation used by the XPS_LL_TEMAC core to transfer transmit and receive Ethernet frame data with the rest of the embedded system.

Functional Description

A LocalLink interface transfers data in one direction only. Each Ethernet interface will use one LocalLink interface for transmit frames and another LocalLink interface for receive frames. If both Ethernet interfaces in an XPS_LL_TEMAC are used, 4 total LocalLink interfaces will be used for data transfer.

The LocalLink interfaces used in this implementation are 32-bits wide, have side-band control signals, and will typically operate with a clock between 100 and 125 MHz.

Data is transferred across the LocalLink in frames which are composed of a header, a payload, and a footer. The payload contains the actual frame data while the header and footer contain mode and control information. The definition of the header and footer is different for the transmit and receive data paths.

For the transmit data path the "Source" will be the embedded system, typically a DMA controller, and the "Destination" will be the XPS_LL_TEMAC. For the receive data path the "Source" will be the XPS_LL_TEMAC and the "Destination" will be the embedded system, typically a DMA controller.

Control signals are used to mark the header, payload, and footer phases of the frame as well as to signal the readiness of the Source and Destination and to indicate which bytes in the 32-bit path contain valid data.

Figure 46 shows an example of the LocalLink waveforms for a transmit Ethernet frame when both Source and Destination are always ready. If either becomes unready during the transfer, the waveform is extended until the ready signal is re-asserted.

Figure 47 shows an example of the LocalLink waveforms for a receive Ethernet frame when both Source and Destination are always ready. If either becomes unready during the transfer, the waveform is extended until the ready signal is re-asserted.

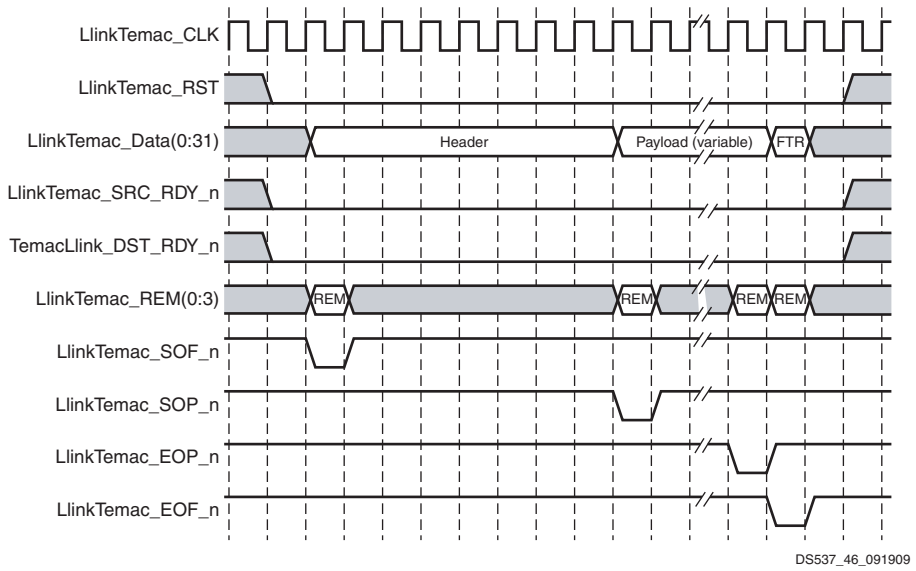

Figure 46: **Typical Waveform of LocalLink Transmit Ethernet Frame**

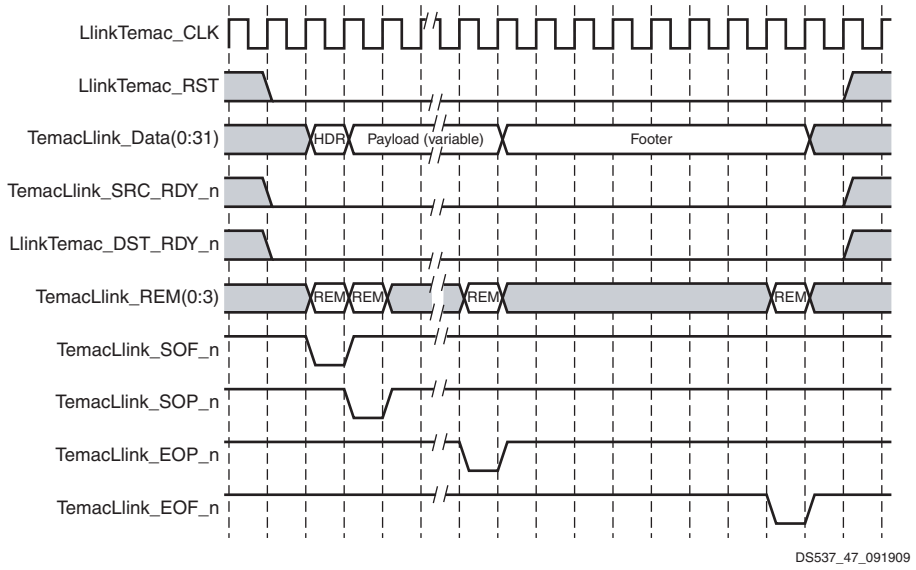

Figure 47: **Typical Waveform of LocalLink Receive Ethernet Frame**

Transmit LocalLink Frame Format

The transmit LocalLink frame always contains eight 32-bit header words (words 0 to 7) and one 32-bit footer word. Of these words, only header words 3, 4, and 5 are used by the XPS_LL_TEMAC. Table 49, Table 50, and Table 51 show the definitions of these words. The footer word is ignored.

If the transmit LocalLink header word 3 bit 31 is "0" (TX_CSCNTRL is disabled) or if the parameter C_TEMAC_TXCSUM is "0" (the transmit checksum off load function is not included in build), then none of the transmit LocalLink header words are used and no transmit checksum off load will take place.

If the parameter C_TEMAC_TXCSUM is "1", then transmit checksum off load can be controlled on a frame by frame basis by setting or clearing the transmit LocalLink Header word 3 bit 31(TX_CSCNTRL).

For more details about how the transmit LocalLink header words are used for transmit checksum off load, please see "TCP/UDP Checksum Off Load in Hardware" on page 75.

The LlinkTemac_REM(0:3) bus is used to indicate how many bytes in the last 32-bit word of the payload are valid data. The bus is used as a mask with a "0" indicating that the byte is valid. For example, LlinkTemac_REM(0:3) = "0111" would indicate that only the first byte of the last word of the payload [LlinkTemac_Data(0:7)] is valid and the remaining three bytes are unused. LlinkTemac_REM(0:3) = "0011" would indicate that the first two bytes of the last word of the payload [LlinkTemac_Data(0:15)] are valid and the remaining two bytes are unused.

Table 49: **Transmit LocalLink Header Word 3 (APP0)**

Bit(s)	Name	Description
(Msb) 0 - 30	Reserved	Undefined value.
31 (Lsb)	TX_CSCNTRL	**Transmit Checksum Enable.** 0 - no transmit checksum off load for this frame 1 - perform transmit checksum off load for this frame if enabled by the C_TEMAC_TXCSUM parameter

Table 50: **Transmit LocalLink Header Word 4 (APP1)**

Bit(s)	Name	Description
(Msb) 0 - 15	TX_CSBEGIN	**Transmit Checksum Calculation Starting Point.** This value is the offset to the location in the frame to the first byte that needs to be included in the checksum calculation. The first byte is indicated by a value of zero. The beginning position must be 16-bit aligned.
16 - 31 (Lsb)	TX_CSINSERT	**Transmit Checksum Insertion Point.** This value is the offset to the location in the frame where the checksum value should be written into the TCP or UDP segment header. The value must be 16-bit aligned and cannot be in the first 8 bytes of the frame.

Table 51: **Transmit LocalLink Header Word 5 (APP2)**

Bit(s)	Name	Description
(Msb) 0 - 15	Reserved	Undefined value.
16 - 31 (Lsb)	TX_CSINIT	**Transmit Checksum Calculation Initial Value.** This value is a 16-bit seed that cane be used to insert the TCP or UDP pseudo header into the checksum calculation. please see "TCP/UDP Checksum Off Load in Hardware" on page 75 for more information on using this field.

Receive LocalLink Frame Format

The receive LocalLink frame always contains one 32-bit header word and eight 32-bit footer words (words 0 to 7). Of these words, only footer words 3 through 7 are populated with values by the XPS_LL_TEMAC. Table 54, Table 55, and Table 56 show the definitions of these words. Reserve fields do not have defined values.

If the parameter C_TEMAC_RXCSUM is “0”, the receive checksum off load function is not included in the build and receive LocalLink footer word 7 will always be zero. If C_TEMAC_RXCSUM is “1”, the raw checksum will be calculated for every frame received and will be placed in receive LocalLink

footer word 7. For more information about using the receive raw checksum value, please see "TCP/UDP Checksum Off Load in Hardware" on page 75.

Receive LocalLink footer word 7 will always contain the number of bytes in length of the frame being sent across the receive LocalLink interface.

The TemacLlink_REM(3:0) bus is used to indicate how many bytes in the last 32-bit word of the payload are valid data. The bus is used as a mask with a "0" indicating that the byte is valid. For example, TemacLlink_REM(0:3) = "0111" would indicate that only the first byte of the last word of the payload [TemacLlink_Data(0:7)] is valid and the remaining three bytes are unused. TemacLlink_REM(0:3) = "0011" would indicate that the first two bytes of the last word of the payload [TemacLlink_Data(0:15)] are valid and the remaining two bytes are unused.

Table 52: **Receive LocalLink Footer Word 3 (APP0)**

Bit(s)	Name	Description
(Msb) 0	STS/CTRL	Undefined value.
1 - 15	Reserved	Undefined value.
16 - 31 (Lsb)	MCAST_ADR_U	**Multicast Address (47:32).** These are the upper 16 bits of the multicast destination address of this frame. This value is only valid if Footer word 5 bit 31 is a 1. The address is ordered so the first byte received is the lowest positioned byte in the register; for example, MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA. This word would be 0xFFEE.

Table 53: **Receive LocalLink Footer Word 4 (APP1)**

Bit(s)	Name	Description
0 - 31	MCAST_ADR_L	**Multicast Address (31:0).** These are the lower 32bits of the multicast destination address of this frame. This value is only valid if Footer word 5 bit 31 is a 1. The address is ordered so the first byte received is the lowest positioned byte in the register; for example, MAC address of AA-BB-CC-DD-EE-FF would be stored in UnicastAddr(47:0) as 0xFFEEDDCCBBAA. This word would be 0xDDCCBBAA.

Table 54: **Receive LocalLink Footer Word 5 (APP2)**

Bit(s)	Name	Description
(Msb) 0 - 28	Reserved	Undefined value.
29	BCAST_FLAG	**Broadcast Frame Flag.** This bit, when 1, indicates that the current frame is a Broadcast frame that has passed the hardware address filtering.
30	IP_MCAST_FLAG	**IP Multicast Frame Flag.** This bit, when 1, indicates that the current frame is a multicast frame that appears to be formed from an IP multicast frame (the first part of the destination address is 01:00:5E) that has passed the hardware multicast address filtering.
31 (Lsb)	MAC_MCAST_FLAG	**MAC Multicast Frame Flag.** This bit, when 1, indicates that the current frame is a MAC multicast frame that has passed the hardware multicast address filtering.

Table 55: **Receive LocalLink Footer Word 6 (APP3)**

Bit(s)	Name	Description
(Msb) 0 - 15	T_L_TPID	**Type Length VLAN TPID.** This is the value of the 13th and 14th bytes of the frame. If the frame is not VLAN type, this will be the type/length field. If the frame is VLAN type, this will be the value of the VLAN TPID field prior to any stripping, translation or tagging.
16 - 31 (Lsb)	RX_CSRAW	**Receive Raw Checksum.** This value is the raw receive checksum calculated over the entire Ethernet frame starting at byte 14. If the receive FCS stripping is not enabled, the FCS will be included in the checksum and must be removed by the application.

Table 56: **Receive LocalLink Footer Word 7 (APP4)**

Bit(s)	Name	Description
(Msb) 0 - 15	VLAN_TAG	**VLAN Priority CFI and VID.** This is the value of the 15th and 16th bytes of the frame. If the frame is VLAN type, this will be the value of the VLAN priority, CFI, and VID fields prior to any stripping, translation, or tagging. If the frame is not VLAN type, this will be the first 2 bytes of the data field.
16 - 17	Reserved	Undefined value.
18- 31 (Lsb)	RX_BYTECNT	**Receive Frame Length (Bytes).** This value is the number of bytes in the Ethernet frame which is in the receive LocalLink payload field.

Mapping Xilinx DMA Buffer Descriptor Fields to LocalLink Fields

The XPS_LL_TEMAC requires that certain LocalLink header and footer fields be used to support TCP / IP Checksum Off load. The XPS_LL_TEMAC does not have any requirements on how the LocalLink fields are created or where the data comes from, only that the correct values are in each field.

At the time that this document is written, Xilinx provides two cores that may be used to provide the required LocalLink functionality to implement TCP / IP Checksum Off load: the SDMA_v2_00_B which is part of the MPMC_V5_04_A and the Hard DMA included in the PowerPC 440 Processor block. Please refer to the their respective documents list in "Reference Documents" on page 155 for more information.

These DMA cores are designed to operate with many LocalLink cores in addition to the XPS_LL_TEMAC so their documents are necessarily general and do not make reference specifically to the data used for TCP/ IP Checksum Off load. This document will briefly show the mapping between how these two core's data maps to the fields in the LocalLink for the purposes of TCP / IP Checksum Off load.

Please note that the information that follows is specific to these two core's implementation at the time that this document is written and that the implementation may change in the future. If the implementation of these two cores does change, this data sheet will not necessarily be updated to show the new implementation.

These DMA cores use registers to point to data areas in external memory called Buffer Descriptors. The Buffer Descriptors are eight 32-bit words in external memory and contain DMA operation control information, pointers to other areas of external memory which contain data to move (DMA) which are called Data Buffers, and generic Application Defined words which map to header and footer fields of the LocalLink bus.

Figure 48 shows the mapping between the DMA Buffer Descriptor words in external memory and the fields in the LocalLink bus for the transmit case and Figure 49 shows the mapping for the receive case.

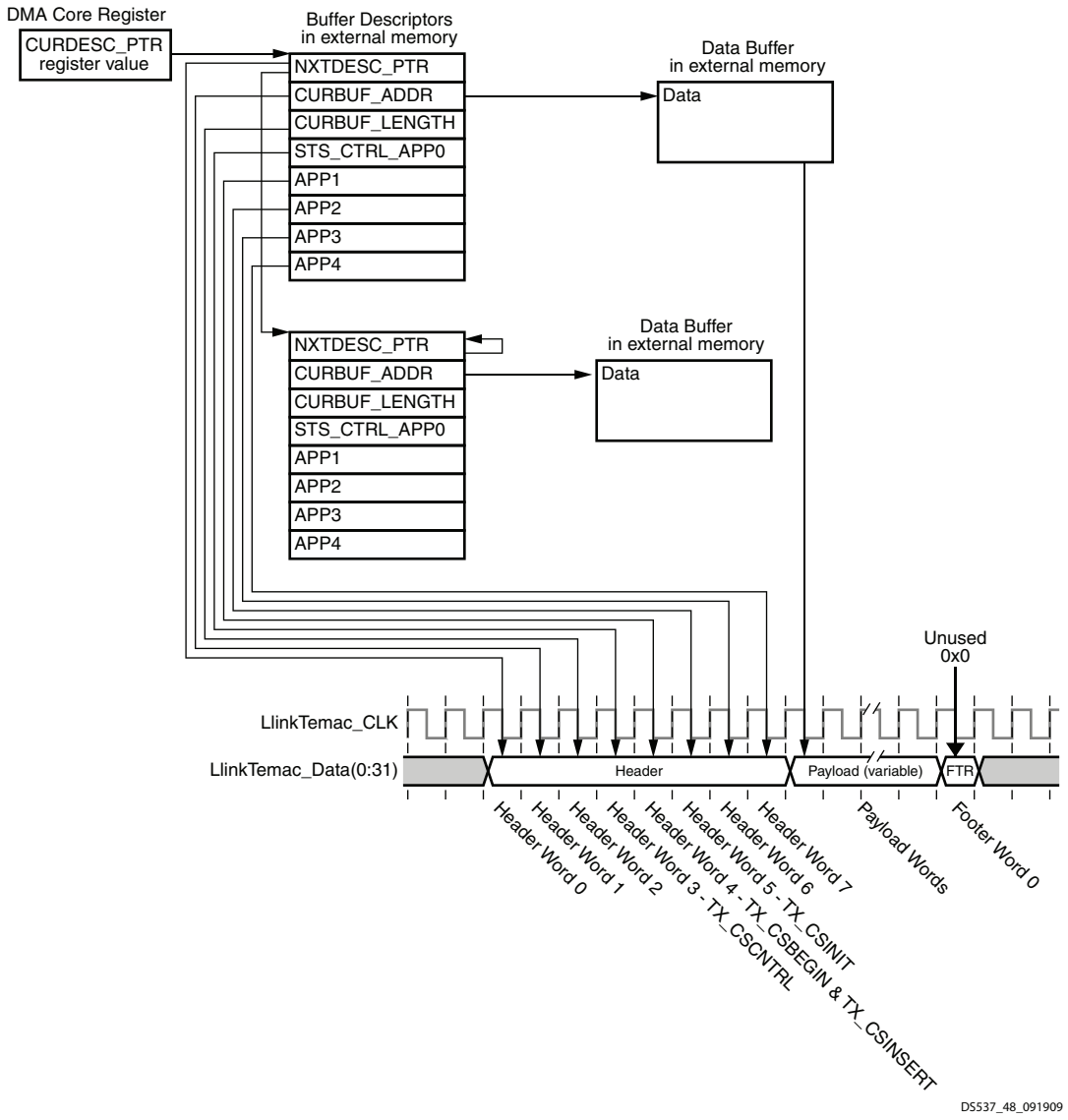

Figure 48: **Transmit DMA Buffer Descriptor LocalLink Field Mapping**

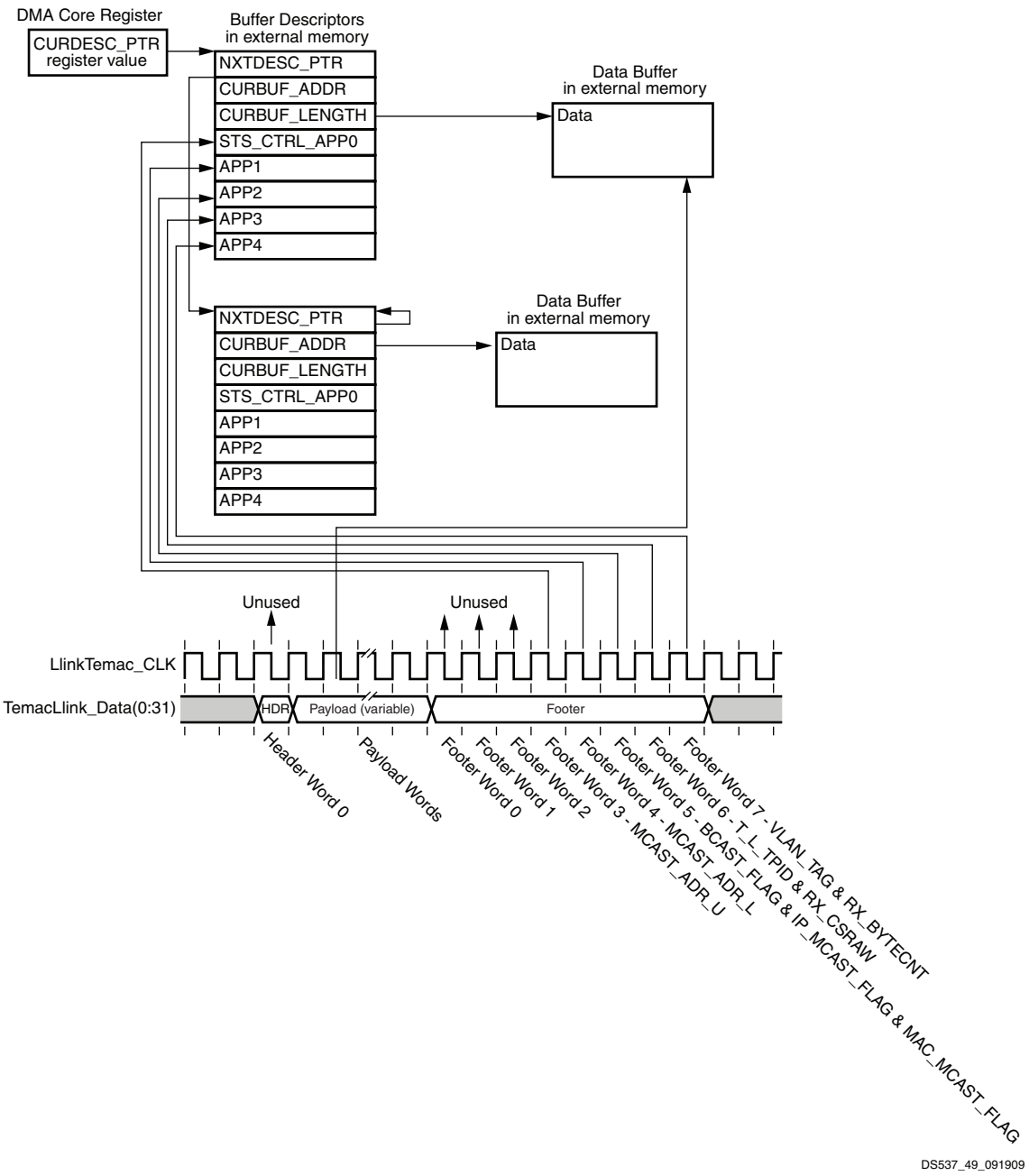

Figure 49: **Receive DMA Buffer Descriptor LocalLink Field Mapping**

Frame Transmission

Padding

When fewer than 46 bytes of data are supplied to the XPS_LL_TEMAC, the transmitter will add padding up to the minimum frame length. However, when the FCS field is being provided as part of the frame by the user, the frame must already be padded if necessary to maintain the minimum frame length.

FCS Pass Through

The XPS_LL_TEMAC can calculate and add the FCS field to each transmitted frame or it can pass through an FCS field supplied with the frame data by the user. When a user supplied FCS field is passed through, the user must supply padding as necessary to ensure that the frame meets the minimum frame length requirement. FCS insertion or pass through is controlled by the TC register bit 29 (page 58).

Virtual LAN (VLAN) Frames

When transmitting VLAN frames (if enabled by the TC register bit 27 page 58) without extended VLAN mode, the user must supply the VLAN type tag 0x8100 a well as the two byte tag control field along with the rest of the frame data. More information about the tag control field is available in the IEEE Std 802.3-2002 specification.

Maximum Frame Length and Jumbo Frames

The maximum length of a frame specified in the IEEE Std 802.3-2002 specification is 1518 bytes for non-VLAN tagged frames. VLAN tagged frames can be extended to 1522 bytes. When jumbo frame handling is disabled (TC register bit 30 page 58) and the user attempts to transmit a frame that exceeds the maximum legal length, the XPS_LL_TEMAC inserts an error code to corrupt the current frame and the frame is truncated to the maximum legal length. When jumbo frame handling is enabled, frames longer then the legal maximum are transmitted error free. Jumbo frames are restricted by the XPS_LL_TEMAC design to less than 16K Bytes.

Frame Reception

Frame Reception with Errors

An unsuccessful frame reception (for example, a fragment frame or a frame with an incorrect FCS) will be dropped and not passed to the user. A Receive Reject interrupt will be activated (see bit 28 in Table 12).

FCS Pass Through or Stripping

If the Length/Type field has a length interpretation, the received frame could be padded to meet the minimum frame size specification. If FCS Pass Through is disabled (RCW1 register bit 29 page 57) and Length/Type filed error checking is enabled (RCW1 register bit 25 page 57), the padding is stripped along with the FCS field and is not passed to the user. If FCS Pass Through is disabled (RCW1 register bit 29 page 57) and Length/Type field error checking is also disabled, the padding is not stripped and is passed to the user but the FCS field is stripped and is not passed to the user.

If the FCS Pass Through is enabled, any padding will be passed to the user along with the FCS field. Even though the FCS is passed up to the user, it is also verified and the frame will be dropped if the FCS is incorrect. A Receive Reject interrupt will be activated (see bit 28 in Table 12).

Table 57: **Receive Frame FCS Field and Pad Field Stripping or Pass Through**

	FCS Pass Through (RCW1 register bit 29 = 1)	FCS Strip (RCW1 register bit 29 = 0)
Length/Type field error check (RCW1 register bit 25 = 0)	FCS and padding (if present) fields passed to user for all accepted frames	FCS and padding (if present) fields stripped and not passed to user for all accepted frames
Length/Type field error ignore (RCW1 register bit 25 = 1)	FCS and padding (if present) fields passed to user for all accepted frames	FCS field stripped and not passed to user but padding (if present) passed to user for all accepted frames

Virtual LAN (VLAN) Frames

Received VLAN tagged frames will be passed to the user if VLAN frame reception is enabled (RCW1 register bit 27 page 57). This is the basic native VLAN support provided by the TEMAC core. For more information about extended VLAN functions, please refer to those sections which follow.

Maximum Frame Length and Jumbo Frames

The maximum length of a frame specified in the IEEE Std 802.3-2002 specification is 1518 bytes for non-VLAN tagged frames. VLAN tagged frames can be extended to 1522 bytes. When jumbo frame handling is disabled (RCW1 register bit 30 page 57) and a received frame exceeds the maximum legal length, the frame is dropped and a Receive Reject interrupt will be activated (see bit 28 in Table 12). When jumbo frame handling is enabled, frames longer then the legal maximum are received in the same way as shorter frames. Jumbo frames are restricted by the XPS_LL_TEMAC design to less than 16K Bytes.

Length/Type Field Error Checks

Length/Type field error checking is specified in IEEE Std 802.3. This functionality must be enabled (RCW1 register bit 25 page 57) to comply with this specification. Disabling Length/Type checking is intended only for specific applications, such as when using over a proprietary backplane.

Enabled

When Length/Type error checking is enabled, the following checks are made on all frames received. (If either of these checks fails, the frame is dropped and a Receive Reject interrupt will be activated (see bit 28 in Table 12).

- A value greater than or equal to decimal 46 but less than decimal 1536 in the length/type field is checked against the actual data length received.
- A value less than decimal 46 in the length/type field is checked to ensure the data field is padded to exactly 46 bytes. The resultant frame is now the minimum frame size: 64 bytes total in length.

Additionally, if FCS passing is disabled, the length/type field will be used to strip the FCS field **AND** any padding that may exist. **NEITHER** will be passed to the user.

Disabled

When the length/type error checking is disabled, the length/type error checking above is not performed and a frame that has only these errors will be accepted.

Additionally, if FCS passing is disabled, the length/type field is **NOT** used to determine padding that may exist and the FCS field **WILL** be stripped but any padding that may exist in the frame **WILL NOT** be stripped and **WILL** be passed to the user.

Address Filtering

Basic Mode

The receive address filtering function accepts or rejects received frames by examining the destination address field. Part of this function is carried out in the Hard TEMAC silicon component and part is carried out based on the bit settings in the Control Register (page 28). Figure 50 shows the address filtering flow. The decisions shown in white are made in the Hard TEMAC silicon component while the decisions shown in grey are made based on the Control Register settings.

The filtering functions includes:

Hard TEMAC Silicon component functions:

- Programmable unicast destination address matching
- Four programmable multicast address matching
- Broadcast address recognition (0xFFFF FFFF FFFF)
- Optional pass through mode with address filter disabled (promiscuous mode)
- Pause control frame address recognition (0x0100 00C2 8001)

Control Register enabled functions:

- Enable or reject received multicast frames
- Enable or reject received broadcast frames

Receive address filtering eliminates the software overhead required to process frames that aren't relevant to a particular Ethernet interface by checking the Destination Address (DA) field of the received frame.

The unicast address and multicast addresses are programmed in software via the PLB bus as are the Address Filter enable bit, Multicast Address enable bit, and Broadcast Address enable bit. The pause frame address and broadcast address are predefined and do not need programming.

Please refer the footnote in Table 12, "Interrupt Status Register Bit Definitions," on page 33 for a more detailed description on the conditions that can cause the receive reject interrupt to be set.

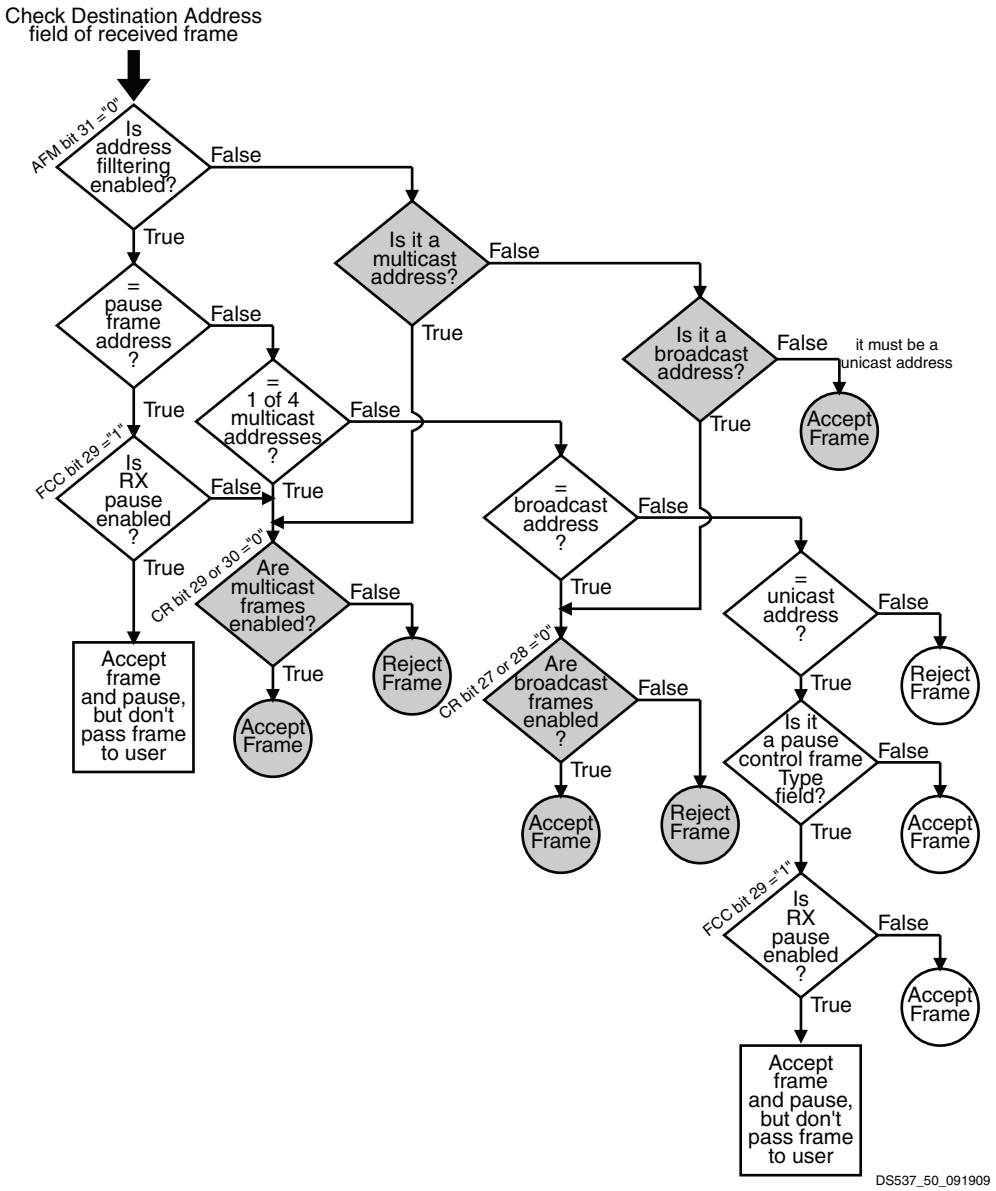

Figure 50: **Receive Address Basic Filtering Flow**

Extended Multicast Address Filtering Mode

General

Currently the hard TEMAC core provides up to 4 multicast addresses that may be specified for receive address validation (i.e., if an incoming multicast frame's receive address matches one of the 4 specified addresses, it is accepted). Some users require the ability to use many more multicast address values to filter receive addresses.

While this could be supported with promiscuous mode and software application filtering, some degree of hardware off loading is desired to reduce processor utilization.

Including extended multicast address filtering at build-time by setting parameters C_TEMACx_MCAST_EXTEND to 1 provides additional logic for address filtering beyond what is built in to the TEMAC core itself.

Unfortunately, the TEMAC core will prevent receiving any multicast frames if they do not match one of the 4 entries in the built-in multicast address table. As a result, the TEMAC core will have to be placed in promiscuous address mode to force it to pass all multicast frames through to the extended multicast address filtering logic.

However, this means it will also pass through all unicast address frames. In order to not increase the processor load for unicast address filtering, additional unicast address filtering will have to be added to the extended multicast address filtering logic. The user must make sure that the TEMAC core is in promiscuous receive address mode when using this extended multicast address filtering mode.

Implementation Details

Received multicast frames that meet all other hardware verification requirements will receive a first level address filtering in hardware. Frames that pass this initial filtering will be passed up to software drivers with information provided by hardware to assist the software drivers in providing the second level/final address filtering. If the frame does not pass hardware filtering, the frame will be dropped and no action will be required by the software drivers.

While a MAC multicast address is defined as any 48 bit MAC address that has bit 0 (LSb) set to 1 (for example 01:00:00:00:00:00), in most cases the MAC multicast address is created from a IP multicast address as shown in Figure 51. It is these IP multicast addresses that are a subset of MAC multicast addresses that are filtered by the extended multicast address filtering mode.

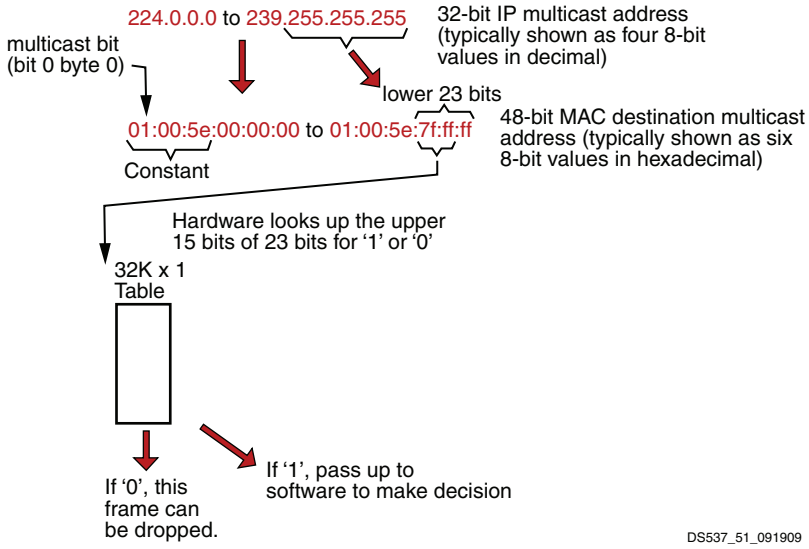

Figure 51: **Mapping IP Multicast Addresses to MAC Multicast Addresses**

When a multicast address frame is received while this extended multicast filtering is enabled, the xps_ll_temac first verifies that the first 24 bits are 01:00:5E and then will use the upper 15 bits of the unique 23 bit MAC multicast address to index this memory. If the associated memory location contains a 1 then the frame is accepted and passed up to software for a comparison on the full 23-bit address. If the memory location is a 0 or the upper 24 bits are not 01:00:5E then the frame is not accepted and it is dropped.

The memory is 1-bit wide but is addressed on 32-bit word boundaries. The memory is 32K deep. This table must be initialized by software via the PLB interface

When using the extended multicast address filtering, the TEMAC must be set to promiscuous mode so that all frames are available for filtering. When doing this the TEMAC no longer checks for a unicast address match. Additional registers "Unicast Address Word Lower Register (UAWL0 and UAWL1)" and "Unicast Address Word Upper Register (UAWU0 and UAWU1)" are available to provide unicast address filtering while in this mode.

For builds that have the extended multicast address filtering enabled, promiscuous mode can be achieved by making sure that the TEMAC is in promiscuous mode and by clearing the EMultiFltrEnbl bit (bit 19) in the "Reset and Address Filter Registers (RAF0 and RAF1)".

When a received frame is accepted and passed up to software, additional information is provided in the receive LocalLink footer words to help the software perform the additional address filtering with less overhead.

Receive LocalLink footer words 3 and 4 include the destination address of the frame and footer word 5 includes bits to indicate if the frame had a destination address that was the broadcast address, a MAC multicast address, or an IP multicast address (and if none of those bits are set, it was a unicast address). Please see the section on "Receive LocalLink Frame Format" for more information.

This allows the software to make decisions about the destination address without accessing the address from within the payload of the LocalLink transfer among the other frame data. When using a Xilinx DMA core, this means the information needed by the software for filtering is in the buffer descriptor and a decision can be made regarding accepting or rejecting the frame without accessing the data buffer itself thus reducing memory access and buffer indexing overhead.

Flow Control

The flow control function is defined by IEEE Std 802.3-2002 Clause 31. The XPS_LL_TEMAC can be configured to send pause frames and to act upon the pause frames received. These two behaviors can be configured independently (asymmetrically). To enable or disable transmit and receive flow control, refer to the FCC register (page 59).

Flow control can be used to prevent data loss when an Ethernet interface is unable to process frames fast enough to keep up with the rate of frames provided by another Ethernet interface. When this occurs, the Ethernet interface that requires relief can transmit a pause control frame to the link partner to request it cease transmitting for a defined period of time.

Transmitting a Pause Control Frame

For the XPS_LL_TEMAC, a pause frame transmission can be initiated by writing a pause value to the TPF register (page 31) while transmit pause processing is enabled (FCC register bit 30 is 1 page 59).

Requesting the transmit of a pause frame will not interrupt a transmission in progress but the pause frame will be transmitted after the frame in progress. A request to transmit a pause frame will result in the transmission of a pause frame even if the transmitter itself is already paused due to the reception of a pause frame.

The destination address supplied with the transmitted pause control frame can be set by writing to the RCW0 and RCW1 registers (page 56).

Receiving a Pause Control Frame

When an error free frame is received by the XPS_LL_TEMAC, it examines the following information:

1. The destination address field is compared to the pause control address and the configured unicast address.
2. The Length/Type field is compared against the control type code (0x8808).
3. The opcode field contents are matched against the pause control opcode (0x0001).

If compare step 2 or 3 fails or if flow control for the receiver is disabled (FCC register bit 29 is 0 page 59), the frame is ignored by the flow control logic and is passed to the user.

If the frames passes all 3 compare steps and receive flow control is enabled, the pause parameter in the frame is used to inhibit transmitter operation for the time defined in the IEEE Std 802.3-2002 specification, a Receive Reject interrupt will be activated (see bit 28 in Table 12), and the frame will not be passed up to software.

If the transmitter is paused and a second pause frame is received, the current pause value of the transmitter is replaced with the new pause value received in the new pause frame including a possible value of 0x0.

Statistics Vectors

Transmit Statistics Vector

The transmitter provides 32 bits of statistics for each frame transmitted as well as a signal which can be used to count the total number of bytes transmitted. The 32-bit value is driven out one bit at a time following the transmission of each frame (shown in Figure 52).

Table 58 shows the bit definition of the transmit statistics. Bits 28 to 20 will always be driven to zero because half-duplex is not supported.

Logic can be used to de-multiplex the transmit statistics.

Table 58: **Transmit Statistics Bit Definitions**

ClientTxStats	Name	Description
31	PAUSE_FRAME_TRANSMITTED	Asserted if the previous frame was a pause frame initiated by writing to the TPF register.
30	Reserved (driven to zero)	Returns 0.
29	Reserved (driven to zero)	Returns 0.
25 - 28	TX_ATTEMPTS (driven to zeros)	Returns 0s because half-duplex is not supported.
24	Reserved (driven to zero)	Returns 0.
23	EXCESSIVE COLLISION (driven to zero)	Returns 0s because half-duplex is not supported.
22	LATE_COLLISION (driven to zero)	Returns 0 because half-duplex is not supported.
21	EXCESSIVE_DEFERRAL (driven to zero)	Returns 0 because half-duplex is not supported.
20	TX_DEFERRED (driven to zero)	Returns 0 because half-duplex is not supported.

Table 58: **Transmit Statistics Bit Definitions**

ClientTxStats	Name	Description
19	VLAN_FRAME	Asserted if the previous frame contains a VLAN identifier in the Length/Type field when transmitter VLAN operation is enabled
5 - 18	FRAME_LENGTH_COUNT	The length of the previous frame in number of bytes. The count sticks at 16838 for jumbo frames larger than this value.
4	CONTROL_FRAME	Asserted if the previous frame has the special Control type code 0x8808 in the Length/Type field
3	UNDERRUN_FRAME	Asserted if the previous frame contains an underrun error.
2	MULTICAST_FRAME	Asserted if the previous frame contains a multicast address in the destination address field.
1	BROADCAST_FRAME	Asserted if the previous frame contains a broadcast address in the destination address field.
0	SUCCESSFUL_FRAME	Asserted if the previous frame is transmitted without error.

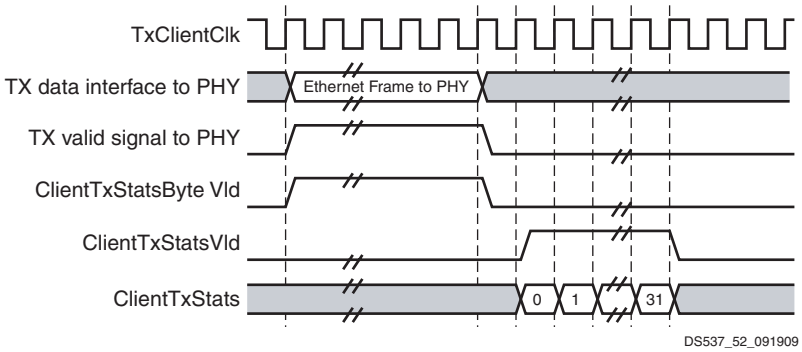

Figure 52: **Transmit Statistics Waveforms**

Receive Statistics Vector

The receiver provides 27 bits of statistics for each frame transmitted as well as a signal which can be used to count the total number of bytes transmitted. The 32-bit value is driven out one bit at a time following the transmission of each frame (shown in Figure 53).

Table 59 shows the bit definition of the receive statistics. Bits 28 to 20 will always be driven to zero because half-duplex is not supported.

Logic can be used to de-multiplex the receive statistics.

Table 59: **Receive Statistics Bit Definitions**

ClientTxStats	Name	Description
26	ALIGNMENT_ERROR	Used in 10/100 MII mode. Asserted if the previous frame received has an incorrect FCS value and a misalignment occurs when the 4-bit MII data bus is converted to the 8-bit GMII data bus.
25	Length/Type Out Of Range	Asserted if the Length/Type field contains a length that does not match the number of data byte received. Also asserted if the Length/Type field indicates that the frame contains padding but the number of data bytes received is not equal to 64 bytes (minimum frame size). The exception is when the Length/Type field error checks are disabled.
24	BAD_OPCODE	Asserted if the previous frame is error free, contains the special control frame identifier in the Length/Type field, but contains an OPCODE unsupported by the XPS_LL_TEMAC (any OPCODE other then Pause).
23	FLOW_CONTROL_FRAME	Asserted if the previous frame is error free. Contains the special control frame identifier in the Length/Type field. Contains a destination address matching either the pause control address or the unicast address. Contains the supported PAIUSE OPCODE and is acted upon by the XPS_LL_TEMAC.
22	Reserved (driven to zero)	Returns 0.
21	VLAN_FRAME	Asserted if the previous frame contains a VLAN identifier in the Length/Type field when the receiver VLAN operation is enabled.
20	OUT_OF_BOUNDS	Asserted if the previous frame exceeded the specified IEEE Std 802.3-2002 maximum legal length. This is only valid if jumbo frames are disabled.
19	CONTROL_FRAME	Asserted if the previous frame contains the special control frame identifier in the Length/Type field.
5 - 18	FRAME_LENGTH_COUNT	The length of the previous frame in number of bytes. The count sticks at 16383 for any jumbo frames larger than this value.
4	MULTICAST_FRAME	Asserted if the previous frame contains a multicast address in the destination field.
3	BROADCAST_FRAME	Asserted if the previous frame contains the broadcast address in the destination field.
2	FCS_ERROR	Asserted if the previous frame received has an incorrect FCS value or the XPS_LL_TEMAC detects error codes during reception.
1	BAD_FRAME(1)	Asserted if the previous frame received contains errors.
0	GOOD_FRAME(1)	Asserted if the previous frame received is error free.

1. If the Length/Type field error checks are disabled, then a frame containing this type of error is marked as a GOOD_FRAME, providing no additional errors are detected.

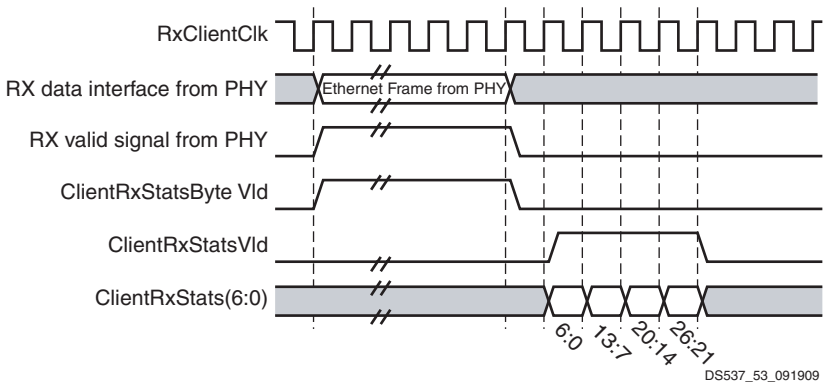

Figure 53: **Receive Statistics Waveforms**

Extended VLAN Support

VLAN General Information

VLAN (or Virtual Local Area Network) frames are used to segregate Ethernet traffic within a larger physical LAN. VLAN frames are created by inserting a four byte VLAN TAG field in an Ethernet frame where the two byte Type/Length field would normally occur thus extending the overall frame by 4 bytes. The VLAN TAG field is further broken down into additional fields as shown in Figure 54.

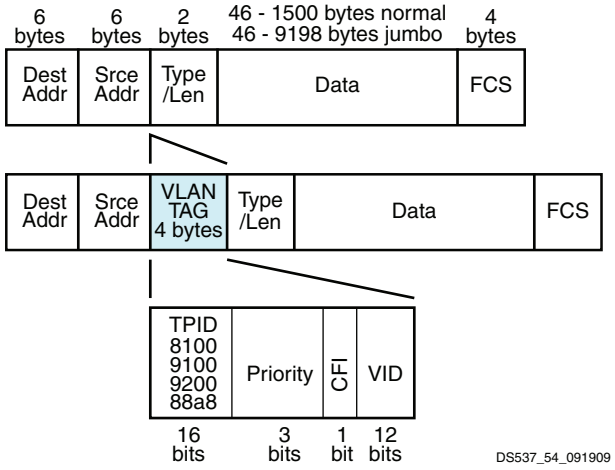

Figure 54: **VLAN Frame Showing VLAN Tag Field**

The TEMAC core provides basic VLAN support that can be enabled or disabled independently. This basic support recognizes VLAN frames that have a TPID value of 0x8100. When basic VLAN function is enabled, the TEMAC core will allow good VLAN frames with this TPID value to be processed for validation and address filtering rather than being dropped.

However, some applications require using a TPID value other than 0x8100 or will have multiple VLAN tags within one frame (referred to as double tagging, triple tagging, etc.). Additionally, some common operations are performed on VLAN frames that can be off-loaded from software to hardware to reduce processor utilization. Some of these tasks, translation, stripping, and auto tagging, are available when

the extended VLAN support is included in the core at build-time by setting the appropriate parameters.

The extended VLAN functions are available individually and independently between the transmit and receive paths.

In order to use the extended VLAN functions, the circuitry must be included at build time by setting the appropriate parameters and also the functions must be enabled at run time by setting the New Functions enable bit (bit 20) of the "Reset and Address Filter Registers (RAF0 and RAF1)".

VLAN Translation

VLAN translation will enable the xps_ll_temac core to replace the VLAN ID (VID) value of the VLAN Tag field of a VLAN frame with a new VID as it passes through the xps_ll_temac core in either the transmit or receive direction.

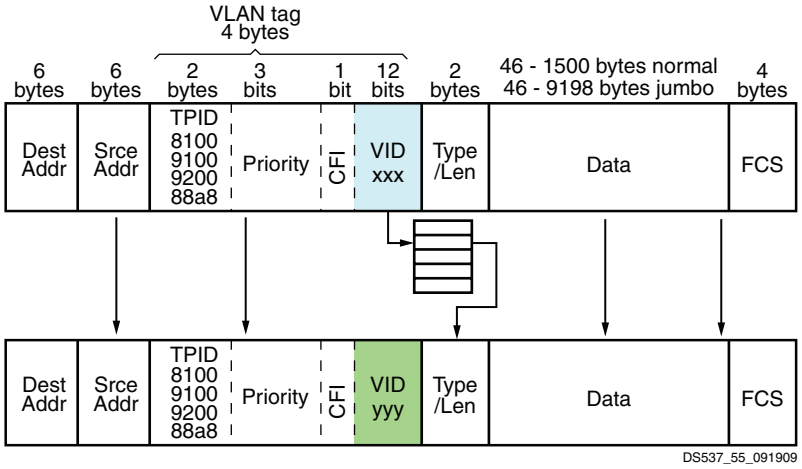

Figure 55: **VLAN VID Translation**

The TEMAC core will not recognize transmitting or receiving VLAN frames with a TPID other than 0x8100 when VLAN mode is enabled. If VLAN mode is disabled, then the maximum length of a normal frame will not be extended from 1518 to 1522 bytes Additionally, multiple tagging is also not supported because of the even larger frame sizes.

To support multiple VLAN tagging and the use of TPID values other than 0x8100 in the outer tag, jumbo frame mode must be used with basic VLAN mode disabled. This will eliminate automatic invalidating (by the TEMAC core) of any frames that normally would be too large for "normal" frame sizes. The user must enable jumbo frame mode and disable VLAN mode when needed for extended VLAN mode.

Transmit Path

When transmitting frames, the outgoing frame is detected as a VLAN frame by recognizing a VLAN Tag Protocol Identifier value (TPID) in the Type/Length field by comparing it against user defined values in the "VLAN TPID Word 0 Register (TPID00 and TPID10)" and "VLAN TPID Word 1 Register (TPID01 and TPID11)". Note that the TPID values are shared between the receive and transmit paths.

Once a VLAN frame is identified, the 12-bit Unique VLAN Identifier (VID) is used to access The "Transmit VLAN Data Table (0 and 1)" to supply a replacement VID value which is substituted into the outgoing frame.

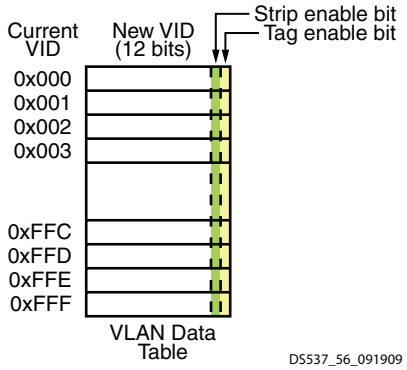

Figure 56: **VLAN Data Table**

Using transmit In-Band FCS mode of the TEMAC core is not allowed when using VLAN translation because the user provided FCS field value would not be correct for the new VID field.

For double, triple, etc. tagged VLAN frames, only the outer VID will be translated.

The following TPID values are commonly used to flag VLAN frames: 0x8100, 0x9100, 0x9200, and 0x88a8 however, the TPID values used to identify VLAN frames are programmable via the TPID registers.

Transmit and receive VLAN translation can be enabled separately with their respective parameters.

For VID values that do not need translated, the VLAN data table location associated with their value must be initialized to that same value.

Receive Path

The receive operates similarly to the transmit side. The frame first passes through address filtering and validation processing before being checked for a VLAN TPID.

Receive FCS stripping in the TEMAC core is required when using VLAN translation because the FCS field that arrives with the frame will no longer be valid with the new TPID value. Please note that although receive stripping is enabled, any padding if present will not be stripped due to the TYPE / LENGTH field of the receive frame containing a VLAN tag rather than a length value.

VLAN Tagging and Double Tagging (Stacking)

VLAN tagging allows the TEMAC to insert a pre-defined VLAN tag in select Ethernet frames as they pass through the core in either the transmit or receive direction.

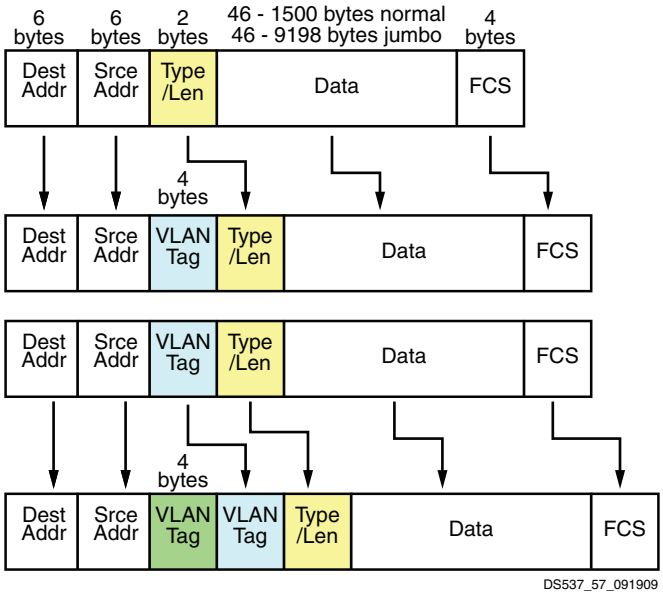

Figure 57: **VLAN Tagging**

General

One VLAN tag will be added depending on mode of operation:

- Non-VLAN frames will get one VLAN tag added to become single VLAN tagged frames.
- VLAN tagged frames will receive another VLAN tag and no checking will be performed to see how many VLAN tags the frame already has (if there are already 3 tags it will now have 4).

Therefore, in cases that require adding a VLAN tag, one VLAN tag will be added to the existing frame.

The TEMAC core's basic VLAN mode extends the maximum normal frame size validation by 4 bytes. This mode does not extend to multiple VLAN tagging. Multiple VLAN frames that exceed 1522 bytes would be discarded as too long. As mentioned previously, this requires the use of jumbo frame mode which will eliminate the automatic invalidation of frames that normally would be too large for "normal" frame sizes.

When VLAN tagging is enabled at build time with the appropriate parameter, a field in the "Reset and Address Filter Registers (RAF0 and RAF1)" will be used to select one of four VLAN tagging modes and the "Transmit VLAN Tag Register (TTAG0 and TTAG1)" and "Receive VLAN Tag Register (RTAG0 and RTAG1)" will be used to hold the VLAN tag value which will be inserted.

The four VLAN tagging modes which are selectable at run time are:

1. Do not add tags to any frames
2. Add one tag to all frames
3. Add one tag only to frames that are already VLAN tagged
4. Add one tag only to select frames that are already VLAN tagged based on VID value

The forth mode requires a method for specifying which tagged frames should receive an additional VLAN tag. The "Transmit VLAN Data Table (0 and 1)" and "Receive VLAN Data Table (0 and 1)" are used for this purpose. A 1 in the tag enable field for a TPID value indicates that frame should receive an additional tag.

Again, transmit In-Band FCS mode is not allowed and receive FCS stripping is required when using VLAN tagging because FCS field value would not be correct for the frame with the additional VLAN tag. Although receive stripping is enabled, any padding if present will not be stripped because the TYPE / LENGTH field of the receive frame contains a VLAN tag rather than a length value. However, the length field is still present.

VLAN Stripping

VLAN stripping allows the TEMAC to remove a VLAN tag in select Ethernet frames as they pass through the xps_ll_temac core in either the transmit or receive direction.

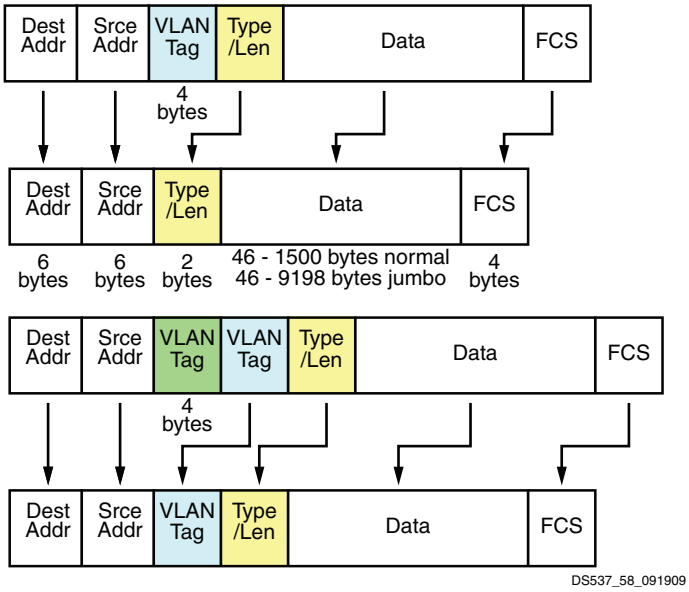

Figure 58: **VLAN Stripping**

General

One VLAN tag will be removed:

- Non-VLAN frames will not be changed
- VLAN tagged frames will have the outer VLAN tag removed and we won't check to see how many VLAN tags it already has (if there are 4 tags we will make it 3).

When VLAN stripping is enabled at build time with the appropriate parameter, a field in the "Reset and Address Filter Registers (RAF0 and RAF1)" will be used to select one of three VLAN stripping modes.

1. Do not strip tags from any frames
2. Strip one tag from all VLAN tagged frames
3. Strip one tag only from select VLAN tagged frames based on VID value

The third mode requires a method for specifying which tagged frames should be stripped. The "Transmit VLAN Data Table (0 and 1)" and "Receive VLAN Data Table (0 and 1)" are used for this purpose. A 1 in the strip enable field for a TPID value indicates that frame should have its VLAN tag stripped.

Again, transmit In-Band FCS mode is not allowed and receive FCS stripping is required when using VLAN stripping because FCS field value would not be correct for the frame with the VLAN tag removed. Please note that although receive stripping is enabled, any padding if present will not be

stripped due to the TYPE / LENGTH field of the receive frame containing a VLAN tag rather than a length value.

Order of VLAN Functions when Combined

When multiple VLAN functions are combined, the order of processing for both transmit and receive shall be:

1. VLAN Stripping
2. VLAN Translation
3. VLAN Tagging

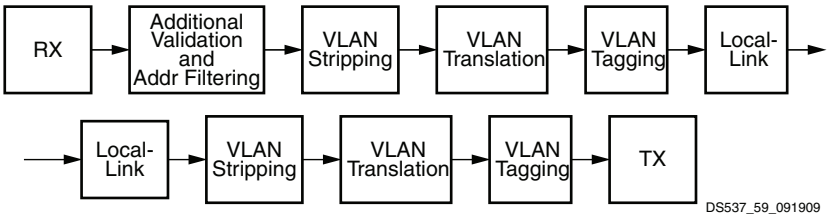

Figure 59: **Order of Extended VLAN Functions**

Ethernet Audio Video Bridging (AVB)

Ethernet AVB functionality is supported with XPS_LL_TEMAC; however, the LogicCORE IP Ethernet AVB Endpoint must be generated as a pcore and manually connected to the XPS_LL_TEMAC with the AVB functionality enabled.

Please refer to UG492 LogicCORE IP Ethernet AVB Endpoint for more information on AVB.

Virtex-6 Hard TEMAC Implementations

Introduction to Physical Interfaces

The Hard TEMAC silicon component in the Virtex-6 FPGA devices is independent of, and can connect to, any type of physical layer device. The XPS_LL_TEMAC provides additional circuitry around the Hard TEMAC silicon component to allow easy use of several common physical layer device interfaces.

The following are two types of physical layer interfaces:

- **BASE-T** provide a link between the XPS_LL_TEMAC and copper mediums. This functionality can be provided in a XPS_LL_TEMAC system by connecting to external BASE_T PHY devices which are readily available. This connection can be made using MII, GMII/MII, RGMII, and SGMII interfaces.
  - Virtex-6 devices support GMII/MII at 2.5 V only.
- **BASE-X** provide a link between the XPS_LL_TEMAC and (usually) fiber optic mediums. The XPS_LL_TEMAC system can provide this function at 1000 Mb/S (1000BASE-X) by using a RocketIO transceiver.

More information will be added as it becomes available.

Media Independent Interface (MII)

The Media Independent Interface (MII), defined in IEEE 802.3 clause 22, is a parallel interface that connects at 10-Mb/S and/or 100-Mb/S to external PHY devices.

The MII design uses clock enables. Please refer to UG368 Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = "1". When the parameter C_INCLUDE_IO = "0", any BUFGs, IBUFGs, IBUFS, and OBUFs are not used.

Virtex 6 Hard TEMAC MII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

Gigabit Media Independent Interface (GMII)

The Gigabit Media Independent Interface (GMII), defined in IEEE 802.3 clause 35, is an extension of the MII used to connect at 1-Gb/S to the PHY devices.

MII can be considered a subset of GMII, and as a result, GMII/MII together can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

When the GMII interface is selected with parameters for the XPS_LL_TEMAC, a GMII/MII interface is used which is capable of all three Ethernet speeds.

The GMII design uses clock enables. Please refer to UG368 Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = "1". One modification has been performed to the receive clock when C_INCLUDE_IO = 1. The XPS_LL_TEMAC design has been modified such that GMII_RX_CLK_0 is not connected to an IODELAY element. It connects directly to the BUFIO and BUFR. This also applies to GMII_RX_CLK_1 when C_TEMAC1_ENABLED=1. When the parameter C_INCLUDE_IO = "0", any IBUFGs, IBUFS, OBUFs, BUFGMUXs, BUFIOs, BUFRs, and IODELAYs are not used.

Virtex 6 Hard TEMAC GMII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

Reduced Gigabit Media Independent Interface (RGMII)

The Reduced Gigabit Media Independent Interface (RGMII) is an alternative to the GMII/MII. RGMII achieves a 50% reduction in the pin count compared with GMII, and is therefore favored over GMII/MII by PCB designers. This is achieved with the use of double-data-rate (DDR) flip-flops.

RGMII can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

For more information on RGMII, refer to the *Hewlett-Packard RGMII Specification, version 1.3 and 2.0.*

The RGMII design uses clock enables. Please refer to UG368 Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = "1" for both RGMII Version 2.0 and RGMII Version 1.3. When the parameter C_INCLUDE_IO = "0", the BUFR, BUFIO and IODELAY on the RGMII_RXC signal are not used.

Virtex 6 Hard TEMAC RGMII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

Serial Gigabit Media Independent Interface (SGMII)

The Serial-GMII (SGMII) is an alternative interface to the GMII/MII that converts the parallel interface of the GMII into a serial format. This radically reduces the I/O count and is therefore often favored by PCB designers. This is achieved by using a RocketIO transceiver.

SGMII can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

The SGMII physical interface was defined by Cisco Systems. The data signals operate at a rate of 1.25 Gb/S. Differential pairs are used to provide signal integrity and minimize noise. The sideband clock signals defined in the specification are not implemented in the XPS_LL_TEMAC. Instead, the RocketIO MGT is used to transmit and receive the differential data at the required rate using clock data recovery. For more information on SGMII, refer to the *Serial GMII Specification v1.7*.

Please refer to UG368 Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = “1”. When the parameter C_INCLUDE_IO = “0”, When the parameter C_INCLUDE_IO = “0”, MGTCLK_P connects directly to the Serial Transceiver; hence the IBUFDS is not used.

Virtex 6 Hard TEMAC SGMII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

SGMII Auto-Negotiation

The external SGMII capable PHY device performs auto negotiation with its link partner on the PHY Link (Ethernet bus) resolving operational speed and duplex mode and then in turn performs a secondary auto negotiation with the RocketIO transceiver across the SGMII Link. This transfers the results of the PHY with Link Partner auto negotiation across the SGMII to the XPS_LL_TEMAC.

The results of the SGMII auto negotiation can be read from the SGMII Management Auto negotiation Link Partner Ability Base Register (Table 79). The duplex mode and speed of the XPS_LL_TEMAC should then be set to match (see "TEMAC Receive Configuration Word 1 (RCW1) Registers" on page 56, "TEMAC Transmit Configuration (TC) Registers" on page 58, and "TEMAC Ethernet MAC Mode Configuration (EMMC) Registers" on page 60).

There are two methods that may be used to learn of the completion of an auto negotiation cycle:

By polling the auto negotiation complete bit of SGMII Management Status Register (Register 1, bit 5 Table 75).

By using the auto negotiation complete interrupt (See "Interrupt Status Registers (IS0 and IS1)" on page 32 and SGMII Management Auto Negotiation Interrupt Control Register Table 84 on page 114.)

Loopback

There are two possible loopback positions:

- **Loopback in the Hard TEMAC silicon component**. When placed into loopback, data is routed from the transmitter to the receiver path at the last possible point in the PCS/PMA sublayer. This is immediately before the RocketIO transceiver interface. When placed into loopback, a constant

stream of Idle code groups is transmitted through the RocketIO transceiver. Loopback in this position allows test frames to be looped back within the system without allowing them to be received by the link partner (the device connected on the other end of the Ethernet. The transmission of Idles allows the link partner to remain in synchronization so that no fault is reported.

- **Loopback in the RocketIO transceiver**. The RocketIO transceiver can be switched into loopback and will route data from the transmitter path to the receiver path within the RocketIO transceiver. However, this data is also transmitted out of the RocketIO transceiver and so any test frames used for a loopback test will be received by the link partner.

Loopback can be enabled or disabled by writing to the SGMII Management Control Register bit 14 (Table 74 on page 110) while the loopback position can be controlled by writing the SGMII Management Loopback Control Register bit 0 (Table 85 on page 114).

1000BASE-X PCS/PMA

Please refer to UG368 Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = “1”. When the parameter C_INCLUDE_IO = “0”, MGTCLK_P connects directly to the Serial Transceiver; hence the IBUFDS is not used.

PCS/PMA

The Physical Coding Sublayer (PCS) for 1000BASE-X operation is defined in IEEE 802.3 clause 36 and 37 and performs the following:

- Encoding (and decoding) of GMII data octets to form a sequence of ordered sets
- 8B/10B encoding (and decoding) of the sequence ordered sets
- 1000BASE-X Auto-Negotiation for information exchange with the link partner

The Physical Medium Attachment (PMA) for 1000BASE-X operation is defined in IEEE 802.3 clause 36 and performs the following:

- Serialization (and de serialization) of code-groups for transmission (and reception) on the underlying serial PMD
- recovery of clock from the 8B/10B coded data supplied by the PMD

1000BASE-X PCS/PMA functionality is provided by connecting the Hard TEMAC silicon component to a RocketIO transceiver.

PMD

The Physical Medium Dependent (PMD) sublayer is defined in IEEE 802.3 clause 38 for 1000BASE-LX and 1000BASE-SX (long and short wave laser). This type of PMD is provided by the external GBIC or SFP optical transceiver which should be connected directly to the ports of the RocketIO transceiver.

Virtex 6 Hard TEMAC 1000BASE-X Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

1000BASE-X Auto-Negotiation

1000BASE-X auto negotiation is described in IEEE Std 802.3, clause 37. This function allows a device to advertise the supported modes of operation to a device at the remote end of a link segment (the link partner on Ethernet), and detect corresponding operational modes advertised by the link partner.

The results of the auto negotiation can be read from the 1000BASE-X Management Auto negotiation Link Partner Ability Base Register (Table 66). The duplex mode and speed of the XPS_LL_TEMAC should then be set to match (see "TEMAC Receive Configuration Word 1 (RCW1) Registers" on page 56, "TEMAC Transmit Configuration (TC) Registers" on page 58, and "TEMAC Ethernet MAC Mode Configuration (EMMC) Registers" on page 60).

There are two methods that may be used to learn of the completion of an auto negotiation cycle:

- By polling the auto negotiation complete bit of 1000BASE-X Management Status Register (Register 1, bit 5 Table 62).

By using the auto negotiation complete interrupt (See "Interrupt Status Registers (IS0 and IS1)" on page 32 and 1000BASE-X Management Auto Negotiation Interrupt Control Register Table 71 on page 108.)

Loopback

There are two possible loopback positions:

- **Loopback in the Hard TEMAC silicon component**. When placed into loopback, data is routed from the transmitter to the receiver path at the last possible point in the PCS/PMA sublayer. This is immediately before the RocketIO transceiver interface. When placed into loopback, a constant stream of Idle code groups is transmitted through the RocketIO transceiver. Loopback in this position allows test frames to be looped back within the system without allowing them to be received by the link partner (the device connected on the other end of the Ethernet. The transmission of Idles allows the link partner to remain in synchronization so that no fault is reported.
- **Loopback in the RocketIO** transceiver. The RocketIO transceiver can be switched into loopback and will route data from the transmitter path to the receiver path within the RocketIO transceiver. However, this data is also transmitted out of the RocketIO transceiver and so any test frames used for a loopback test will be received by the link partner.

Loopback can be enabled or disabled by writing to the 1000BASE-X Management Control Register bit 14 (Table 61 on page 103) while the loopback position can be controlled by writing the 1000BASE-X Management Loopback Control Register bit 0 (Table 72 on page 109).

Internal 1000BASE-X PCS/PMA Management Registers

Registers 0 through 15 are defined in IEEE 802.3. These registers contain information relating to the operation of the 1000BASE-X PCS/PMA sublayer, including the status of the physical Ethernet link (PHY Link).

Additionally, these registers are directly involved in the operation of the 1000BASE-X auto negotiation function which occurs between the XPS_LL_TEMAC and its link partner, the Ethernet device connected at the far end of the PHY Link.

These registers are accessed via the MII Management interface (See "Using the MII Management to Access Internal or External PHY Registers" on page 73). These registers are only valid when using the 1000BASE-X PHY interface.

When using 1000BASE-X, the XPS_LL_TEMAC is typically connected to an external optical transceiver device such as a GBIC or SFP transceiver.

Table 60: **Internal 1000BASE-X PCS/PMA Management Registers**

Register Name	Register Address (REGAD)
Control Register (Register 0)	0
Status Register (Register 1)	1
PHY Identifier (Register 2 and 3)	2,3
Auto Negotiation Advertisement Register (Register 4)	4
Auto Negotiation Link Partner Ability Base Register (Register 5)	5
Auto Negotiation Expansion Register (Register 6)	6
Auto Negotiation Next Page Transmit Register (Register 7)	7
Auto Negotiation Next Page Receive Register (Register 8)	8
Extended Status Register (Register 15)	15
Vendor Specific Register: Auto Negotiation Interrupt Control Register (Register 16)	16
Vendor Specific Register: Loopback Control Register (Register 17)	17

Table 61 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Control Register bit definitions.

Table 61: **1000BASE-X Management Control Register (Register 0) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Reset	Read/Write self clearing	0	0 - normal operation 1 - PCS/PMA reset
14	Loopback	Read/Write	0	0 - disable loopback mode 1 - enable loopback mode
13	Speed Selection (LSB)	Returns 0	0	Always returns 0 for this bit. Along with bit 6, speed selection of 1000 Mb/S is identified.
12	Auto Negotiation Enable	Read/Write	1	0 - disable auto negotiation 1 - enable auto negotiation
11	Power Down	Read/Write	0	When set to "1", the RocketIO MGT is placed in a low power state. This bit requires a reset (bit 15) to clear. 0 - normal operation 1 - power down
10	Isolate	Read/Write	0	0 - normal operation 1 - electrically isolate the PHY
9	Restart Auto Negotiation	Read/Write self clearing	0	0 - normal operation 1 - restart auto negotiation process

Table 61: **1000BASE-X Management Control Register (Register 0) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
8	Duplex Mode	Returns 1	1	Always returns 1 for this bit to disable COL test.
7	Collision Test	Returns 0	0	Always returns 0 for this bit to signal full duplex mode.
6	Speed Selection (MSB)	Returns 1	1	Always returns 1 for this bit. Along with bit 13, speed selection of 1000 Mb/S is identified.
5	Unidirectional Enable	Read/Write	0	Enable transmit regardless of whether a valid link has been established.
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 62 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Status Register bit definitions.

Table 62: **1000BASE-X Management Status Register (Register 1) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	100BASE-T4	Returns 0	0	Always returns a 0 for this bit because 100BASE-T4 is not supported.
14	100BASE-X Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X full duplex is not supported.
13	100BASE-X Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X half duplex is not supported.
12	10 Mb/S Full Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S full duplex is not supported.
11	10 Mb/S Half Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S half duplex is not supported.
10	100BASE-T2 Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 full duplex is not supported.
9	100BASE-T2 Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 half duplex is not supported.
8	Extended Status	Returns 1	1	Always returns a 1 for this bit indicating the presence of the extended register (register 15).
7	Unidirectional Ability	Returns 1	1	Always returns a 1.
6	MF Preamble Suppression	Returns 1	1	Always returns a 1 for this bit to indicate the support of management frame preamble suppression.
5	Auto Negotiation Complete	Read	0	0 - auto negotiation process not completed 1 - auto negotiation process complete
4	Remote Fault	Read only self clearing on read	0	0 - no remote fault condition detected 1 - remote fault condition detected
3	Auto Negotiation Ability	Returns 1	1	Always returns a q for this bit indicating that the PHY is capable of auto negotiation.

Table 62: **1000BASE-X Management Status Register (Register 1) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
2	Link Status	Read only self clearing on read	0	0 - PHY Link is down 1 - PHY Link is up
1	Jabber Detect	Returns 0	0	Always returns a 0 for this bit because no jabber detect is supported.
0	Extended Capability	Returns 0	0	Always returns a 0 for this bit because no extended register set is supported.

Table 63 shows the first Hard TEMAC Internal 1000BASE-X PCS/PMA Management PHY Identifier Register bit definitions.

Table 63: **1000BASE-X Management PHY Identifier (Register 2) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	OUI	Read	returns OUI (3-18) 0x0028	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.

Table 64 shows the second Hard TEMAC Internal 1000BASE-X PCS/PMA Management PHY Identifier Register bit definitions.

Table 64: **1000BASE-X Management PHY Identifier (Register 3) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
10 - 15	OUI	Read	returns OUI (19-24) 0x0035	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.
30	MMN	Returns 0	0	Manufacturer's Model Number. Always returns 0s.
29	Revision	Returns 0	0	Revision Number. Always returns 0s.

Table 65 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Advertisement Register bit definitions.

Table 65: **1000BASE-X Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/Write	0	0 - next page functionality is not advertised 1 - next page functionality is advertised
14	Reserved	Returns 0s	0	Always return zeros.
12 - 13	Remote Fault	Read/Write self clearing after auto negotiation	0x0	00 - no error 01 - offline 10 - link failure 11 - auto negotiation error
9 - 11	Reserved	Returns 0s	0x0	Always return zeros.

Table 65: **1000BASE-X Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
7 - 8	Pause	Read/write	0x3	00 - no pause 01 - asymmetric pause towards link partner 10 - symmetric pause 11 - both symmetric pause and asymmetric pause towards link partner
6	Half Duplex	Returns 0	0	Always return zeros because half duplex is not supported.
5	Full Duplex	Read/Write	1	0 - full duplex mode is not advertised 1 - full duplex mode is advertised
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 66 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto negotiation Link Partner Ability Base Register bit definitions.

Table 66: **1000BASE-X Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - next page functionality is not supported 1 - next page functionality is supported
14	Acknowledge	Read	0	Used by the auto negotiation function to indicate reception of a link partner's base or next page.
12 - 13	Remote Fault	Read/	0x0	00 - no error 01 - offline 10 - link failure 11 - auto negotiation error
9 - 11	Reserved	Returns 0s	0x0	Always return zeros.
7 - 8	Pause	Read	0x	00 - no pause 01 - asymmetric pause supported 10 - symmetric pause supported 11 - both symmetric pause and asymmetric pause supported
6	Half Duplex	Read	0	0 - half duplex mode is not supported 1 - half duplex mode is supported
5	Full Duplex	Read/	0	0 - full duplex mode is not supported 1 - full duplex mode is supported
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 67 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto negotiation Expansion Register bit definitions.

Table 67: **1000BASE-X Management Auto Negotiation Expansion Register (Register 6) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
3 - 15	Reserved	Returns 0s	0x0	Always return zeros.
2	Next Page Able	Returns 1	1	Always returns a 1 for this bit because the device is Next Page Able.
1	Page Received	Read self clearing on read	0	0 - a new page is not received 1 - a new page is received
0	Reserved	Returns 0s	0	Always return zeros.

Table 68 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Next Page Transmit Register bit definitions.

Table 68: **1000BASE-X Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/Write	0	0 - last page 1 - additional next page(s) will follow
14	Reserved	Returns 0s	0	Always return zeros.
13	Message Page	Read/Write	1	0 - unformatted page 1 - message page
12	Acknowledge 2	Read/Write	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read/Write	0x001 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 69 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Next Page Receive Register bit definitions.

Table 69: **1000BASE-X Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - last page 1 - additional next page(s) will follow
14	Acknowledge	Read	0	Used by auto negotiation function to indicate reception of a link partner's base or next page.
13	Message Page	Read	0	0 - unformatted page 1 - message page

Table 69: **1000BASE-X Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
12	Acknowledge 2	Read	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read	0x0 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 70 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Extended Status Register bit definitions.

Table 70: **1000BASE-X Management Extended Status Register (Register 15) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	1000BASE-X Full Duplex	Returns 1	1	Always returns a 1 for this bit because 1000BASE-X full duplex is supported.
14	1000BASE-X Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-X half duplex is not supported.
13	1000BASE-T Full Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T full duplex is not supported.
12	1000BASE-T Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T half duplex is not supported.
0 - 11	Reserved	Returns 0s	0x0	Always return zeros.

Table 71 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Interrupt Control Register bit definitions.

Table 71: **1000BASE-X Management Auto Negotiation Interrupt Control Register (Register 16) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
2 - 15	Reserved	Returns 0s	0	Always return zeros.
1	Interrupt Status	Read/Write	0	If the interrupt is enabled, this bit will be asserted upon the completion of an auto negotiation cycle; it will only be cleared by writing 0 to this bit. If the interrupt is disabled, this bit will be set to 0. This is the auto negotiation complete interrupt. 0 - interrupt is asserted 1 - interrupt is not asserted
0	Interrupt Enable	Read/Write	1	0 - interrupt is disabled 1 - interrupt is enabled

Table 72 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Loopback Control Register bit definitions.

Table 72: **1000BASE-X Management Loopback Control Register (Register 17) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
1 - 15	Reserved	Returns 0s	0	Always return zeros.
0	Loopback Position	Read/Write	0	Loopback is enabled or disabled using register 0 bit 14. 0 - loopback (when enabled) occurs directly before the interface to the RocketIO transceiver 1 - loopback (when enabled) occurs in the RocketIO transceiver

Internal SGMII Management Registers

Registers 0 through 15 are defined in IEEE 802.3. These registers contain information relating to the operation of the SGMII PCS sublayer, including the status of both the SGMII Link and the physical Ethernet link (PHY Link).

Additionally, these registers are directly involved in the operation of the SGMII auto negotiation function which occurs between the XPS_LL_TEMAC and the external PHY device (typically a tri-speed BASE-T PHY).

These registers are accessed via the MII Management interface (See "Using the MII Management to Access Internal or External PHY Registers" on page 73). These registers are only valid when using the SGMII PHY interface.

Table 73: **Internal SGMII Management Registers**

Register Name	Register Address (REGAD)
SGMII Control Register (Register 0)	0
SGMII Status Register (Register 1)	1
SGMII PHY Identifier (Register 2 and 3)	2,3
SGMII Auto Negotiation Advertisement Register (Register 4)	4
SGMII Auto Negotiation Link Partner Ability Base Register (Register 5)	5
SGMII Auto Negotiation Expansion Register (Register 6)	6
SGMII Auto Negotiation Next Page Transmit Register (Register 7)	7
SGMII Auto Negotiation Next Page Receive Register (Register 8)	8
SGMII Extended Status Register (Register 15)	15
SGMII Vendor Specific Register: Auto Negotiation Interrupt Control Register (Register 16)	16
SGMII Vendor Specific Register: Loopback Control Register (Register 17)	17

Table 74 shows the Hard TEMAC Internal SGMII PCS Management Control Register bit definitions.

Table 74: **SGMII Management Control Register (Register 0) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Reset	Read/Write self clearing	0	0 - normal operation 1 - PCS/PMA reset
14	Loopback	Read/Write	0	0 - disable loopback mode 1 - enable loopback mode
13	Speed Selection (LSB)	Returns 0	0	Always returns 0 for this bit. Along with bit 6, speed selection of 1000 Mb/S is identified.
12	Auto Negotiation Enable	Read/Write	1	0 - disable auto negotiation 1 - enable auto negotiation
11	Power Down	Read/Write	0	When set to "1", the RocketIO MGT is placed in a low power state. This bit requires a reset (bit 15) to clear. 0 - normal operation 1 - power down
10	Isolate	Read/Write	0	0 - normal operation 1 - electrically isolate the PHY
9	Restart Auto Negotiation	Read/Write self clearing	0	0 - normal operation 1 - restart auto negotiation process
8	Duplex Mode	Returns 1	1	Always returns 1 for this bit to disable COL test.
7	Collision Test	Returns 0	0	Always returns 0 for this bit to signal full duplex mode.
6	Speed Selection (MSB)	Returns 1	1	Always returns 1 for this bit. Along with bit 13, speed selection of 1000 Mb/S is identified.
5	Unidirectional Enable	Read/Write	0	Enable transmit regardless of whether a valid link has been established.
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 75 shows the Hard TEMAC Internal SGMII PCS Management Status Register bit definitions.

Table 75: **SGMII Management Status Register (Register 1) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	100BASE-T4	Returns 0	0	Always returns a 0 for this bit because 100BASE-T4 is not supported.
14	100BASE-X Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X full duplex is not supported.
13	100BASE-X Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X half duplex is not supported.
12	10 Mb/S Full Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S full duplex is not supported.
11	10 Mb/S Half Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S half duplex is not supported.

Table 75: **SGMII Management Status Register (Register 1) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
10	100BASE-T2 Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 full duplex is not supported.
9	100BASE-T2 Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 half duplex is not supported.
8	Extended Status	Returns 1	1	Always returns a 1 for this bit indicating the presence of the extended register (register 15).
7	Unidirectional Ability	Returns 1	1	Always returns a 1.
6	MF Preamble Suppression	Returns 1	1	Always returns a 1 for this bit to indicate the support of management frame preamble suppression.
5	Auto Negotiation Complete	Read	0	0 - auto negotiation process not completed 1 - auto negotiation process complete
4	Remote Fault	Read only self clearing on read	0	0 - no remote fault condition detected 1 - remote fault condition detected
3	Auto Negotiation Ability	Returns 1	1	Always returns a q for this bit indicating that the PHY is capable of auto negotiation.
2	Link Status	Read only self clearing on read	0	0 - PHY Link is down 1 - PHY Link is up
1	Jabber Detect	Returns 0	0	Always returns a 0 for this bit because no jabber detect is supported.
0	Extended Capability	Returns 0	0	Always returns a 0 for this bit because no extended register set is supported.

Table 76 shows the first Hard TEMAC Internal SGMII PCS Management PHY Identifier Register bit definitions.

Table 76: **SGMII Management PHY Identifier (Register 2) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	OUI	Read	returns OUI (3-18) 0x0028	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.

Table 77 shows the second Hard TEMAC Internal SGMII PCS Management PHY Identifier Register bit definitions.

Table 77: **SGMII Management PHY Identifier (Register 3) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
10 - 15	OUI	Read	returns OUI (19-24) 0x0035	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.
30	MMN	Returns 0	0	Manufacturer's Model Number. Always returns 0s.
29	Revision	Returns 0	0	Revision Number. Always returns 0s.

Table 78 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Advertisement Register bit definitions.

Table 78: **SGMII Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	All bits	Read	0x0001	SGMII defined value sent from the MAC to the PHY.

Table 79 shows the Hard TEMAC Internal SGMII PCS Management Auto negotiation Link Partner Ability Base Register bit definitions.

Table 79: **SGMII Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	PHY Link Status	Read	1	This refers to the link status of the external PHY device with its Link Partner across the PHY Link. 0 - link down 1 - link up
14	Acknowledge	Read	0	Used by the auto negotiation function to indicate reception of a link partner's base or next page.
13	Reserved	Returns 0	0	Always return zero.
12	Duplex Mode	Read	0	The resolved duplex mode that the external PHY device has auto negotiated with its Link Partner across the PHY Link. 0 - half duplex 1 - full duplex
10 - 11	Speed	Read	0x0	The resolved operating speed that the external PHY device has auto negotiated with its Link Partner across the PHY Link. 00 - 10 Mb/S 01 - 100 Mb/S 10 -1000 Mb/S 11 - Reserved
1 - 9	Reserved	Returns 0s	0x0	Always return zeros.
0	Reserved	Returns 1	1	Always return one.

Table 80 shows the Hard TEMAC Internal SGMII PCS Management Auto negotiation Expansion Register bit definitions.

Table 80: **SGMII Management Auto Negotiation Expansion Register (Register 6) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
3 - 15	Reserved	Returns 0s	0x0	Always return zeros.
2	Next Page Able	Returns 1	1	Always returns a 1 for this bit because the device is Next Page Able.
1	Page Received	Read self clearing on read	0	0 - a new page is not received 1 - a new page is received
0	Reserved	Returns 0s	0	Always return zeros.

Table 81 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Next Page Transmit Register bit definitions.

Table 81: **SGMII Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/write	0	0 - last page 1 - additional next page(s) will follow
14	Reserved	Returns 0s	0	Always return zeros.
13	Message Page	Read/Write	1	0 - unformatted page 1 - message page
12	Acknowledge 2	Read/Write	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read/Write	0x001 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 82 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Next Page Receive Register bit definitions.

Table 82: **SGMII Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - last page 1 - additional next page(s) will follow
14	Acknowledge	Read	0	Used by auto negotiation function to indicate reception of a link partner's base or next page.
13	Message Page	Read	0	0 - unformatted page 1 - message page
12	Acknowledge 2	Read	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read	0x0 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 83 shows the Hard TEMAC Internal SGMII PCS Management Extended Status Register bit definitions.

Table 83: **SGMII Management Extended Status Register (Register 15) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	1000BASE-X Full Duplex	Returns 1	1	Always returns a 1 for this bit because 1000BASE-X full duplex is supported.
14	1000BASE-X Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-X half duplex is not supported.
13	1000BASE-T Full Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T full duplex is not supported.
12	1000BASE-T Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T half duplex is not supported.
0 - 11	Reserved	Returns 0s	0x0	Always return zeros.

Table 84 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Interrupt Control Register bit definitions.

Table 84: **SGMII Management Auto Negotiation Interrupt Control Register (Register 16) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
2 - 15	Reserved	Returns 0s	0	Always return zeros.
1	Interrupt Status	Read/Write	0	If the interrupt is enabled, this bit will be asserted upon the completion of an auto negotiation cycle; it will only be cleared by writing 0 to this bit. If the interrupt is disabled, this bit will be set to 0. This is the auto negotiation complete interrupt. 0 - interrupt is asserted 1 - interrupt is not asserted
0	Interrupt Enable	Read/Write	1	0 - interrupt is disabled 1 - interrupt is enabled

Table 85 shows the Hard TEMAC Internal SGMII PCS Management Loopback Control Register bit definitions.

Table 85: **SGMII Management Loopback Control Register (Register 17) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
1 - 15	Reserved	Returns 0s	0	Always return zeros.
0	Loopback Position	Read/Write	0	Loopback is enabled or disabled using register 0 bit 14. 0 - loopback (when enabled) occurs directly before the interface to the RocketIO transceiver 1 - loopback (when enabled) occurs in the RocketIO transceiver

Virtex-5 Hard TEMAC Implementations

Introduction to Physical Interfaces

The Hard TEMAC silicon component in the Virtex-5 FPGA devices is independent of, and can connect to, any type of physical layer device. The XPS_LL_TEMAC provides additional circuitry around the Hard TEMAC silicon component to allow easy use of several common physical layer device interfaces.

The following are two types of physical layer interfaces:

- **BASE-T** provide a link between the XPS_LL_TEMAC and copper mediums. This functionality can be provided in a XPS_LL_TEMAC system by connecting to external BASE_T PHY devices which are readily available. This connection can be made using MII, GMII/MII, RGMII, and SGMII interfaces.
  - Virtex-5 devices support GMII/MII at 3.3 V or lower.
- **BASE-X** provide a link between the XPS_LL_TEMAC and (usually) fiber optic mediums. The XPS_LL_TEMAC system can provide this function at 1000 Mb/S (1000BASE-X) by using a RocketIO transceiver.

Media Independent Interface (MII)

The Media Independent Interface (MII), defined in IEEE 802.3 clause 22, is a parallel interface that connects at 10-Mb/S and/or 100-Mb/S to external PHY devices.

The MII design uses clock enables. Please refer to UG194 Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = “1”. When the parameter C_INCLUDE_IO = “0”, any BUFGs, IBUFGs, IBUFS, and OBUFs are not used.

Virtex 5 Hard TEMAC MII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

Gigabit Media Independent Interface (GMII)

The Gigabit Media Independent Interface (GMII), defined in IEEE 802.3 clause 35, is an extension of the MII used to connect at 1-Gb/S to the PHY devices.

MII can be considered a subset of GMII, and as a result, GMII/MII together can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

When the GMII interface is selected with parameters for the XPS_LL_TEMAC, a GMII/MII interface is used which is capable of all three Ethernet speeds.

The GMII design uses clock enables. Please refer to UG194 Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = “1”. When the parameter C_INCLUDE_IO = “0”, any BUFGs, IBUFGs, IBUFS, OBUFs, BUFGMUXs, and IDELAYs are not used.

Virtex 5 Hard TEMAC GMII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

Reduced Gigabit Media Independent Interface (RGMII)

The Reduced Gigabit Media Independent Interface (RGMII) is an alternative to the GMII/MII. RGMII achieves a 50% reduction in the pin count compared with GMII, and is therefore favored over GMII/MII by PCB designers. This is achieved with the use of double-data-rate (DDR) flip-flops.

RGMII can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

For more information on RGMII, refer to the *Hewlett-Packard RGMII Specification, version 1.3 and 2.0.*

The RGMII design uses clock enables. Please refer to UG194 Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = "1" for both RGMII Version 2.0 and RGMII Version 1.3. When the parameter C_INCLUDE_IO = "0", the BUFG and IDELAY on the RGMII_RXC signal are not used.

Virtex 5 Hard TEMAC RGMII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

Serial Gigabit Media Independent Interface (SGMII)

The Serial-GMII (SGMII) is an alternative interface to the GMII/MII that converts the parallel interface of the GMII into a serial format. This radically reduces the I/O count and is therefore often favored by PCB designers. This is achieved by using a RocketIO transceiver.

SGMII can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

The SGMII physical interface was defined by Cisco Systems. The data signals operate at a rate of 1.25 Gb/S. Differential pairs are used to provide signal integrity and minimize noise. The sideband clock signals defined in the specification are not implemented in the XPS_LL_TEMAC. Instead, the RocketIO MGT is used to transmit and receive the differential data at the required rate using clock data recovery. For more information on SGMII, refer to the *Serial GMII Specification v1.7*.

Please refer to UG194 Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = "1". When the parameter C_INCLUDE_IO = "0", When the parameter C_INCLUDE_IO = "0", MGTCLK_P connects directly to the RocketIO GTP/GTX; hence the IBUFDS is not used.

Virtex 5 Hard TEMAC SGMII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

SGMII Auto-Negotiation

The external SGMII capable PHY device performs auto negotiation with its link partner on the PHY Link (Ethernet bus) resolving operational speed and duplex mode and then in turn performs a secondary auto negotiation with the RocketIO transceiver across the SGMII Link. This transfers the results of the PHY with Link Partner auto negotiation across the SGMII to the XPS_LL_TEMAC.

The results of the SGMII auto negotiation can be read from the SGMII Management Auto negotiation Link Partner Ability Base Register (Table 105). The duplex mode and speed of the XPS_LL_TEMAC should then be set to match (see "TEMAC Receive Configuration Word 1 (RCW1) Registers" on page 56,

"TEMAC Transmit Configuration (TC) Registers" on page 58, and "TEMAC Ethernet MAC Mode Configuration (EMMC) Registers" on page 60).

There are two methods that may be used to learn of the completion of an auto negotiation cycle:

By polling the auto negotiation complete bit of SGMII Management Status Register (Register 1, bit 5 Table 101).

By using the auto negotiation complete interrupt (See "Interrupt Status Registers (IS0 and IS1)" on page 32 and SGMII Management Auto Negotiation Interrupt Control Register Table 110 on page 130.)

Loopback

There are two possible loopback positions:

- **Loopback in the Hard TEMAC silicon component**. When placed into loopback, data is routed from the transmitter to the receiver path at the last possible point in the PCS/PMA sublayer. This is immediately before the RocketIO transceiver interface. When placed into loopback, a constant stream of Idle code groups is transmitted through the RocketIO transceiver. Loopback in this position allows test frames to be looped back within the system without allowing them to be received by the link partner (the device connected on the other end of the Ethernet. The transmission of Idles allows the link partner to remain in synchronization so that no fault is reported.
- **Loopback in the RocketIO transceiver**. The RocketIO transceiver can be switched into loopback and will route data from the transmitter path to the receiver path within the RocketIO transceiver. However, this data is also transmitted out of the RocketIO transceiver and so any test frames used for a loopback test will be received by the link partner.

Loopback can be enabled or disabled by writing to the SGMII Management Control Register bit 14 (Table 100 on page 126) while the loopback position can be controlled by writing the SGMII Management Loopback Control Register bit 0 (Table 111 on page 130).

1000BASE-X PCS/PMA

Please refer to UG194 Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = “1”. When the parameter C_INCLUDE_IO = “0”, MGTCLK_P connects directly to the RocketIO GTP/GTX; hence the IBUFDS is not used.

PCS/PMA

The Physical Coding Sublayer (PCS) for 1000BASE-X operation is defined in IEEE 802.3 clause 36 and 37 and performs the following:

- Encoding (and decoding) of GMII data octets to form a sequence of ordered sets
- 8B/10B encoding (and decoding) of the sequence ordered sets
- 1000BASE-X Auto-Negotiation for information exchange with the link partner

The Physical Medium Attachment (PMA) for 1000BASE-X operation is defined in IEEE 802.3 clause 36 and performs the following:

- Serialization (and de serialization) of code-groups for transmission (and reception) on the underlying serial PMD
- recovery of clock from the 8B/10B coded data supplied by the PMD

1000BASE-X PCS/PMA functionality is provided by connecting the Hard TEMAC silicon component to a RocketIO transceiver.

PMD

The Physical Medium Dependent (PMD) sublayer is defined in IEEE 802.3 clause 38 for 1000BASE-LX and 1000BASE-SX (long and short wave laser). This type of PMD is provided by the external GBIC or SFP optical transceiver which should be connected directly to the ports of the RocketIO transceiver.

Virtex 5 Hard TEMAC 1000BASE-X Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

1000BASE-X Auto-Negotiation

1000BASE-X auto negotiation is described in IEEE Std 802.3, clause 37. This function allows a device to advertise the supported modes of operation to a device at the remote end of a link segment (the link partner on Ethernet), and detect corresponding operational modes advertised by the link partner.

The results of the auto negotiation can be read from the 1000BASE-X Management Auto negotiation Link Partner Ability Base Register (Table 92). The duplex mode and speed of the XPS_LL_TEMAC should then be set to match (see "TEMAC Receive Configuration Word 1 (RCW1) Registers" on page 56, "TEMAC Transmit Configuration (TC) Registers" on page 58, and "TEMAC Ethernet MAC Mode Configuration (EMMC) Registers" on page 60).

There are two methods that may be used to learn of the completion of an auto negotiation cycle:

- By polling the auto negotiation complete bit of 1000BASE-X Management Status Register (Register 1, bit 5 Table 88).

By using the auto negotiation complete interrupt (See "Interrupt Status Registers (IS0 and IS1)" on page 32 and 1000BASE-X Management Auto Negotiation Interrupt Control Register Table 97 on page 124.)

Loopback

There are two possible loopback positions:

- **Loopback in the Hard TEMAC silicon component**. When placed into loopback, data is routed from the transmitter to the receiver path at the last possible point in the PCS/PMA sublayer. This is immediately before the RocketIO transceiver interface. When placed into loopback, a constant stream of Idle code groups is transmitted through the RocketIO transceiver. Loopback in this position allows test frames to be looped back within the system without allowing them to be received by the link partner (the device connected on the other end of the Ethernet. The transmission of Idles allows the link partner to remain in synchronization so that no fault is reported.
- **Loopback in the RocketIO** transceiver. The RocketIO transceiver can be switched into loopback and will route data from the transmitter path to the receiver path within the RocketIO transceiver. However, this data is also transmitted out of the RocketIO transceiver and so any test frames used for a loopback test will be received by the link partner.

Loopback can be enabled or disabled by writing to the 1000BASE-X Management Control Register bit 14 (Table 87 on page 119) while the loopback position can be controlled by writing the 1000BASE-X Management Loopback Control Register bit 0 (Table 98 on page 125).

Internal 1000BASE-X PCS/PMA Management Registers

Registers 0 through 15 are defined in IEEE 802.3. These registers contain information relating to the operation of the 1000BASE-X PCS/PMA sublayer, including the status of the physical Ethernet link (PHY Link).

Additionally, these registers are directly involved in the operation of the 1000BASE-X auto negotiation function which occurs between the XPS_LL_TEMAC and its link partner, the Ethernet device connected at the far end of the PHY Link.

These registers are accessed via the MII Management interface (See "Using the MII Management to Access Internal or External PHY Registers" on page 73). These registers are only valid when using the 1000BASE-X PHY interface.

When using 1000BASE-X, the XPS_LL_TEMAC is typically connected to an external optical transceiver device such as a GBIC or SFP transceiver.

Table 86: **Internal 1000BASE-X PCS/PMA Management Registers**

Register Name	Register Address (REGAD)
Control Register (Register 0)	0
Status Register (Register 1)	1
PHY Identifier (Register 2 and 3)	2,3
Auto Negotiation Advertisement Register (Register 4)	4
Auto Negotiation Link Partner Ability Base Register (Register 5)	5
Auto Negotiation Expansion Register (Register 6)	6
Auto Negotiation Next Page Transmit Register (Register 7)	7
Auto Negotiation Next Page Receive Register (Register 8)	8
Extended Status Register (Register 15)	15
Vendor Specific Register: Auto Negotiation Interrupt Control Register (Register 16)	16
Vendor Specific Register: Loopback Control Register (Register 17)	17

Table 87 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Control Register bit definitions.

Table 87: **1000BASE-X Management Control Register (Register 0) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Reset	Read/Write self clearing	0	0 - normal operation 1 - PCS/PMA reset
14	Loopback	Read/Write	0	0 - disable loopback mode 1 - enable loopback mode
13	Speed Selection (LSB)	Returns 0	0	Always returns 0 for this bit. Along with bit 6, speed selection of 1000 Mb/S is identified.
12	Auto Negotiation Enable	Read/Write	1	0 - disable auto negotiation 1 - enable auto negotiation

Table 87: **1000BASE-X Management Control Register (Register 0) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
11	Power Down	Read/Write	0	When set to "1", the RocketIO MGT is placed in a low power state. This bit requires a reset (bit 15) to clear. 0 - normal operation 1 - power down
10	Isolate	Read/Write	0	0 - normal operation 1 - electrically isolate the PHY
9	Restart Auto Negotiation	Read/Write self clearing	0	0 - normal operation 1 - restart auto negotiation process
8	Duplex Mode	Returns 1	1	Always returns 1 for this bit to disable COL test.
7	Collision Test	Returns 0	0	Always returns 0 for this bit to signal full duplex mode.
6	Speed Selection (MSB)	Returns 1	1	Always returns 1 for this bit. Along with bit 13, speed selection of 1000 Mb/S is identified.
5	Unidirectional Enable	Read/Write	0	Enable transmit regardless of whether a valid link has been established.
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 88 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Status Register bit definitions.

Table 88: **1000BASE-X Management Status Register (Register 1) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	100BASE-T4	Returns 0	0	Always returns a 0 for this bit because 100BASE-T4 is not supported.
14	100BASE-X Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X full duplex is not supported.
13	100BASE-X Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X half duplex is not supported.
12	10 Mb/S Full Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S full duplex is not supported.
11	10 Mb/S Half Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S half duplex is not supported.
10	100BASE-T2 Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 full duplex is not supported.
9	100BASE-T2 Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 half duplex is not supported.
8	Extended Status	Returns 1	1	Always returns a 1 for this bit indicating the presence of the extended register (register 15).
7	Unidirectional Ability	Returns 1	1	Always returns a 1.
6	MF Preamble Suppression	Returns 1	1	Always returns a 1 for this bit to indicate the support of management frame preamble suppression.

Table 88: **1000BASE-X Management Status Register (Register 1) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
5	Auto Negotiation Complete	Read	0	0 - auto negotiation process not completed 1 - auto negotiation process complete
4	Remote Fault	Read only self clearing on read	0	0 - no remote fault condition detected 1 - remote fault condition detected
3	Auto Negotiation Ability	Returns 1	1	Always returns a q for this bit indicating that the PHY is capable of auto negotiation.
2	Link Status	Read only self clearing on read	0	0 - PHY Link is down 1 - PHY Link is up
1	Jabber Detect	Returns 0	0	Always returns a 0 for this bit because no jabber detect is supported.
0	Extended Capability	Returns 0	0	Always returns a 0 for this bit because no extended register set is supported.

Table 89 shows the first Hard TEMAC Internal 1000BASE-X PCS/PMA Management PHY Identifier Register bit definitions.

Table 89: **1000BASE-X Management PHY Identifier (Register 2) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	OUI	Read	returns OUI (3-18) 0x0028	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.

Table 90 shows the second Hard TEMAC Internal 1000BASE-X PCS/PMA Management PHY Identifier Register bit definitions.

Table 90: **1000BASE-X Management PHY Identifier (Register 3) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
10 - 15	OUI	Read	returns OUI (19-24) 0x0035	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.
30	MMN	Returns 0	0	Manufacturer's Model Number. Always returns 0s.
29	Revision	Returns 0	0	Revision Number. Always returns 0s.

Table 91 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Advertisement Register bit definitions.

Table 91: **1000BASE-X Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/Write	0	0 - next page functionality is not advertised 1 - next page functionality is advertised
14	Reserved	Returns 0s	0	Always return zeros.

Table 91: **1000BASE-X Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
12 - 13	Remote Fault	Read/Write self clearing after auto negotiation	0x0	00 - no error 01 - offline 10 - link failure 11 - auto negotiation error
9 - 11	Reserved	Returns 0s	0x0	Always return zeros.
7 - 8	Pause	Read/write	0x3	00 - no pause 01 - asymmetric pause towards link partner 10 - symmetric pause 11 - both symmetric pause and asymmetric pause towards link partner
6	Half Duplex	Returns 0	0	Always return zeros because half duplex is not supported.
5	Full Duplex	Read/Write	1	0 - full duplex mode is not advertised 1 - full duplex mode is advertised
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 92 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto negotiation Link Partner Ability Base Register bit definitions.

Table 92: **1000BASE-X Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - next page functionality is not supported 1 - next page functionality is supported
14	Acknowledge	Read	0	Used by the auto negotiation function to indicate reception of a link partner's base or next page.
12 - 13	Remote Fault	Read/	0x0	00 - no error 01 - offline 10 - link failure 11 - auto negotiation error
9 - 11	Reserved	Returns 0s	0x0	Always return zeros.
7 - 8	Pause	Read	0x	00 - no pause 01 - asymmetric pause supported 10 - symmetric pause supported 11 - both symmetric pause and asymmetric pause supported
6	Half Duplex	Read	0	0 - half duplex mode is not supported 1 - half duplex mode is supported
5	Full Duplex	Read/	0	0 - full duplex mode is not supported 1 - full duplex mode is supported
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 93 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto negotiation Expansion Register bit definitions.

Table 93: **1000BASE-X Management Auto Negotiation Expansion Register (Register 6) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
3 - 15	Reserved	Returns 0s	0x0	Always return zeros.
2	Next Page Able	Returns 1	1	Always returns a 1 for this bit because the device is Next Page Able.
1	Page Received	Read self clearing on read	0	0 - a new page is not received 1 - a new page is received
0	Reserved	Returns 0s	0	Always return zeros.

Table 94 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Next Page Transmit Register bit definitions.

Table 94: **1000BASE-X Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/Write	0	0 - last page 1 - additional next page(s) will follow
14	Reserved	Returns 0s	0	Always return zeros.
13	Message Page	Read/Write	1	0 - unformatted page 1 - message page
12	Acknowledge 2	Read/Write	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read/Write	0x001 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 95 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Next Page Receive Register bit definitions.

Table 95: **1000BASE-X Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - last page 1 - additional next page(s) will follow
14	Acknowledge	Read	0	Used by auto negotiation function to indicate reception of a link partner's base or next page.
13	Message Page	Read	0	0 - unformatted page 1 - message page

Table 95: **1000BASE-X Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
12	Acknowledge 2	Read	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read	0x0 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 96 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Extended Status Register bit definitions.

Table 96: **1000BASE-X Management Extended Status Register (Register 15) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	1000BASE-X Full Duplex	Returns 1	1	Always returns a 1 for this bit because 1000BASE-X full duplex is supported.
14	1000BASE-X Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-X half duplex is not supported.
13	1000BASE-T Full Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T full duplex is not supported.
12	1000BASE-T Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T half duplex is not supported.
0 - 11	Reserved	Returns 0s	0x0	Always return zeros.

Table 97 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Interrupt Control Register bit definitions.

Table 97: **1000BASE-X Management Auto Negotiation Interrupt Control Register (Register 16) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
2 - 15	Reserved	Returns 0s	0	Always return zeros.
1	Interrupt Status	Read/Write	0	If the interrupt is enabled, this bit will be asserted upon the completion of an auto negotiation cycle; it will only be cleared by writing 0 to this bit. If the interrupt is disabled, this bit will be set to 0. This is the auto negotiation complete interrupt. 0 - interrupt is asserted 1 - interrupt is not asserted
0	Interrupt Enable	Read/Write	1	0 - interrupt is disabled 1 - interrupt is enabled

Table 98 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Loopback Control Register bit definitions.

Table 98: **1000BASE-X Management Loopback Control Register (Register 17) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
1 - 15	Reserved	Returns 0s	0	Always return zeros.
0	Loopback Position	Read/Write	0	Loopback is enabled or disabled using register 0 bit 14. 0 - loopback (when enabled) occurs directly before the interface to the RocketIO transceiver 1 - loopback (when enabled) occurs in the RocketIO transceiver

Internal SGMII Management Registers

Registers 0 through 15 are defined in IEEE 802.3. These registers contain information relating to the operation of the SGMII PCS sublayer, including the status of both the SGMII Link and the physical Ethernet link (PHY Link).

Additionally, these registers are directly involved in the operation of the SGMII auto negotiation function which occurs between the XPS_LL_TEMAC and the external PHY device (typically a tri-speed BASE-T PHY).

These registers are accessed via the MII Management interface (See "Using the MII Management to Access Internal or External PHY Registers" on page 73). These registers are only valid when using the SGMII PHY interface.

Table 99: **Internal SGMII Management Registers**

Register Name	Register Address (REGAD)
SGMII Control Register (Register 0)	0
SGMII Status Register (Register 1)	1
SGMII PHY Identifier (Register 2 and 3)	2,3
SGMII Auto Negotiation Advertisement Register (Register 4)	4
SGMII Auto Negotiation Link Partner Ability Base Register (Register 5)	5
SGMII Auto Negotiation Expansion Register (Register 6)	6
SGMII Auto Negotiation Next Page Transmit Register (Register 7)	7
SGMII Auto Negotiation Next Page Receive Register (Register 8)	8
SGMII Extended Status Register (Register 15)	15
SGMII Vendor Specific Register: Auto Negotiation Interrupt Control Register (Register 16)	16
SGMII Vendor Specific Register: Loopback Control Register (Register 17)	17

Table 100 shows the Hard TEMAC Internal SGMII PCS Management Control Register bit definitions.

Table 100: **SGMII Management Control Register (Register 0) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Reset	Read/Write self clearing	0	0 - normal operation 1 - PCS/PMA reset
14	Loopback	Read/Write	0	0 - disable loopback mode 1 - enable loopback mode
13	Speed Selection (LSB)	Returns 0	0	Always returns 0 for this bit. Along with bit 6, speed selection of 1000 Mb/S is identified.
12	Auto Negotiation Enable	Read/Write	1	0 - disable auto negotiation 1 - enable auto negotiation
11	Power Down	Read/Write	0	When set to "1", the RocketIO MGT is placed in a low power state. This bit requires a reset (bit 15) to clear. 0 - normal operation 1 - power down
10	Isolate	Read/Write	0	0 - normal operation 1 - electrically isolate the PHY
9	Restart Auto Negotiation	Read/Write self clearing	0	0 - normal operation 1 - restart auto negotiation process
8	Duplex Mode	Returns 1	1	Always returns 1 for this bit to disable COL test.
7	Collision Test	Returns 0	0	Always returns 0 for this bit to signal full duplex mode.
6	Speed Selection (MSB)	Returns 1	1	Always returns 1 for this bit. Along with bit 13, speed selection of 1000 Mb/S is identified.
5	Unidirectional Enable	Read/Write	0	Enable transmit regardless of whether a valid link has been established.
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 101 shows the Hard TEMAC Internal SGMII PCS Management Status Register bit definitions.

Table 101: **SGMII Management Status Register (Register 1) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	100BASE-T4	Returns 0	0	Always returns a 0 for this bit because 100BASE-T4 is not supported.
14	100BASE-X Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X full duplex is not supported.
13	100BASE-X Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X half duplex is not supported.
12	10 Mb/S Full Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S full duplex is not supported.
11	10 Mb/S Half Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S half duplex is not supported.

Table 101: **SGMII Management Status Register (Register 1) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
10	100BASE-T2 Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 full duplex is not supported.
9	100BASE-T2 Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 half duplex is not supported.
8	Extended Status	Returns 1	1	Always returns a 1 for this bit indicating the presence of the extended register (register 15).
7	Unidirectional Ability	Returns 1	1	Always returns a 1.
6	MF Preamble Suppression	Returns 1	1	Always returns a 1 for this bit to indicate the support of management frame preamble suppression.
5	Auto Negotiation Complete	Read	0	0 - auto negotiation process not completed 1 - auto negotiation process complete
4	Remote Fault	Read only self clearing on read	0	0 - no remote fault condition detected 1 - remote fault condition detected
3	Auto Negotiation Ability	Returns 1	1	Always returns a q for this bit indicating that the PHY is capable of auto negotiation.
2	Link Status	Read only self clearing on read	0	0 - PHY Link is down 1 - PHY Link is up
1	Jabber Detect	Returns 0	0	Always returns a 0 for this bit because no jabber detect is supported.
0	Extended Capability	Returns 0	0	Always returns a 0 for this bit because no extended register set is supported.

Table 102 shows the first Hard TEMAC Internal SGMII PCS Management PHY Identifier Register bit definitions.

Table 102: **SGMII Management PHY Identifier (Register 2) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	OUI	Read	returns OUI (3-18) 0x0028	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.

Table 103 shows the second Hard TEMAC Internal SGMII PCS Management PHY Identifier Register bit definitions.

Table 103: **SGMII Management PHY Identifier (Register 3) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
10 - 15	OUI	Read	returns OUI (19-24) 0x0035	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.
30	MMN	Returns 0	0	Manufacturer's Model Number. Always returns 0s.
29	Revision	Returns 0	0	Revision Number. Always returns 0s.

Table 104 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Advertisement Register bit definitions.

Table 104: **SGMII Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	All bits	Read	0x0001	SGMII defined value sent from the MAC to the PHY.

Table 105 shows the Hard TEMAC Internal SGMII PCS Management Auto negotiation Link Partner Ability Base Register bit definitions.

Table 105: **SGMII Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	PHY Link Status	Read	1	This refers to the link status of the external PHY device with its Link Partner across the PHY Link. 0 - link down 1 - link up
14	Acknowledge	Read	0	Used by the auto negotiation function to indicate reception of a link partner's base or next page.
13	Reserved	Returns 0	0	Always return zero.
12	Duplex Mode	Read	0	The resolved duplex mode that the external PHY device has auto negotiated with its Link Partner across the PHY Link. 0 - half duplex 1 - full duplex
10 - 11	Speed	Read	0x0	The resolved operating speed that the external PHY device has auto negotiated with its Link Partner across the PHY Link. 00 - 10 Mb/S 01 - 100 Mb/S 10 -1000 Mb/S 11 - Reserved
1 - 9	Reserved	Returns 0s	0x0	Always return zeros.
0	Reserved	Returns 1	1	Always return one.

Table 106 shows the Hard TEMAC Internal SGMII PCS Management Auto negotiation Expansion Register bit definitions.

Table 106: **SGMII Management Auto Negotiation Expansion Register (Register 6) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
3 - 15	Reserved	Returns 0s	0x0	Always return zeros.
2	Next Page Able	Returns 1	1	Always returns a 1 for this bit because the device is Next Page Able.

Table 106: **SGMII Management Auto Negotiation Expansion Register (Register 6) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
1	Page Received	Read self clearing on read	0	0 - a new page is not received 1 - a new page is received
0	Reserved	Returns 0s	0	Always return zeros.

Table 107 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Next Page Transmit Register bit definitions.

Table 107: **SGMII Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/write	0	0 - last page 1 - additional next page(s) will follow
14	Reserved	Returns 0s	0	Always return zeros.
13	Message Page	Read/Write	1	0 - unformatted page 1 - message page
12	Acknowledge 2	Read/Write	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read/Write	0x001 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 108 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Next Page Receive Register bit definitions.

Table 108: **SGMII Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - last page 1 - additional next page(s) will follow
14	Acknowledge	Read	0	Used by auto negotiation function to indicate reception of a link partner's base or next page.
13	Message Page	Read	0	0 - unformatted page 1 - message page
12	Acknowledge 2	Read	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read	0x0 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 109 shows the Hard TEMAC Internal SGMII PCS Management Extended Status Register bit definitions.

Table 109: **SGMII Management Extended Status Register (Register 15) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	1000BASE-X Full Duplex	Returns 1	1	Always returns a 1 for this bit because 1000BASE-X full duplex is supported.
14	1000BASE-X Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-X half duplex is not supported.
13	1000BASE-T Full Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T full duplex is not supported.
12	1000BASE-T Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T half duplex is not supported.
0 - 11	Reserved	Returns 0s	0x0	Always return zeros.

Table 110 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Interrupt Control Register bit definitions.

Table 110: **SGMII Management Auto Negotiation Interrupt Control Register (Register 16) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
2 - 15	Reserved	Returns 0s	0	Always return zeros.
1	Interrupt Status	Read/Write	0	If the interrupt is enabled, this bit will be asserted upon the completion of an auto negotiation cycle; it will only be cleared by writing 0 to this bit. If the interrupt is disabled, this bit will be set to 0. This is the auto negotiation complete interrupt. 0 - interrupt is asserted 1 - interrupt is not asserted
0	Interrupt Enable	Read/Write	1	0 - interrupt is disabled 1 - interrupt is enabled

Table 111 shows the Hard TEMAC Internal SGMII PCS Management Loopback Control Register bit definitions.

Table 111: **SGMII Management Loopback Control Register (Register 17) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
1 - 15	Reserved	Returns 0s	0	Always return zeros.
0	Loopback Position	Read/Write	0	Loopback is enabled or disabled using register 0 bit 14. 0 - loopback (when enabled) occurs directly before the interface to the RocketIO transceiver 1 - loopback (when enabled) occurs in the RocketIO transceiver

Virtex-4 Hard TEMAC Implementations

Introduction to Physical Interfaces

The Hard TEMAC silicon component in the Virtex-4 FPGA devices is independent of, and can connect to, any type of physical layer device. The XPS_LL_TEMAC provides additional circuitry around the Hard TEMAC silicon component to allow easy use of several common physical layer device interfaces.

The following are two types of physical layer interfaces:

- **BASE-T** provide a link between the XPS_LL_TEMAC and copper mediums. This functionality can be provided in a XPS_LL_TEMAC system by connecting to external BASE_T PHY devices which are readily available. This connection can be made using MII, GMII/MII, RGMII, and SGMII interfaces.
  - Virtex-4 devices support GMII/MII at 3.3 V or lower.
- **BASE-X** provide a link between the XPS_LL_TEMAC and (usually) fiber optic mediums. The XPS_LL_TEMAC system can provide this function at 1000 Mb/S (1000BASE-X) by using a RocketIO transceiver.

Media Independent Interface (MII)

The Media Independent Interface (MII), defined in IEEE 802.3 clause 22, is a parallel interface that connects at 10-Mb/S and/or 100-Mb/S to external PHY devices.

Please refer to UG074 *Virtex-4 FPGA Embedded Tri-Mode Ethernet MAC User Guide v1.9* for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = "1". When the parameter C_INCLUDE_IO = "0", any BUFGs, IBUFGs, IBUFS, and OBUFs are not used. The MII design does not use clock enables.

Virtex 4 Hard TEMAC MII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

Gigabit Media Independent Interface (GMII)

The Gigabit Media Independent Interface (GMII), defined in IEEE 802.3 clause 35, is an extension of the MII used to connect at 1-Gb/S to the PHY devices.

MII can be considered a subset of GMII, and as a result, GMII/MII together can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

When the GMII interface is selected with parameters for the XPS_LL_TEMAC, a GMII/MII interface is used which is capable of all three Ethernet speeds.

Please refer to UG074 *Virtex-4 FPGA Embedded Tri-Mode Ethernet MAC User Guide v1.9* for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = "1". When the parameter C_INCLUDE_IO = "0", any BUFGs, IBUFGs, IBUFS, OBUFs, BUFGMUXs, and IDELAYs are not used. Independent of the C_INCLUDE_IO parameter, a register stage has been inserted before the ODDR registers on the GMII_TXD, GMII_TX_EN, and GMII_TX_ER signals.

Virtex 4 Hard TEMAC GMII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

Reduced Gigabit Media Independent Interface (RGMII)

The Reduced Gigabit Media Independent Interface (RGMII) is an alternative to the GMII/MII. RGMII achieves a 50% reduction in the pin count compared with GMII, and is therefore favored over GMII/MII by PCB designers. This is achieved with the use of double-data-rate (DDR) flip-flops.

RGMII can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

For more information on RGMII, refer to the *Hewlett-Packard RGMII Specification, version 2.0.*

Please refer to UG074 *Virtex-4 FPGA Embedded Tri-Mode Ethernet MAC User Guide v1.9* for an equivalent diagram of the clock management scheme when the XPS_LL_TEMAC parameter C_INCLUDE_IO = "1" for both RGMII Version 2.0 and RGMII Version 1.3. When the parameter C_INCLUDE_IO = "0", the BUFG and IDELAY on the RGMII_RXC signal are not used.

Virtex 4 Hard TEMAC RGMII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

Serial Gigabit Media Independent Interface (SGMII)

The Serial-GMII (SGMII) is an alternative interface to the GMII/MII that converts the parallel interface of the GMII into a serial format. This radically reduces the I/O count and is therefore often favored by PCB designers. This is achieved by using a RocketIO transceiver.

SGMII can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

The SGMII physical interface was defined by Cisco Systems. The data signals operate at a rate of 1.25 Gb/S. Differential pairs are used to provide signal integrity and minimize noise. The sideband clock signals defined in the specification are not implemented in the XPS_LL_TEMAC. Instead, the RocketIO MGT is used to transmit and receive the differential data at the required rate using clock data recovery. For more information on SGMII, refer to the *Serial GMII Specification v1.7*.

Please refer to the UG074 *Virtex-4 FPGA Embedded Tri-Mode Ethernet MAC User Guide v1.9* for an equivalent diagram of the clock management scheme.

Virtex 4 Hard TEMAC SGMII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

SGMII Auto-Negotiation

The external SGMII capable PHY device performs auto negotiation with its link partner on the PHY Link (Ethernet bus) resolving operational speed and duplex mode and then in turn performs a secondary auto negotiation with the RocketIO transceiver across the SGMII Link. This transfers the results of the PHY with Link Partner auto negotiation across the SGMII to the XPS_LL_TEMAC.

The results of the SGMII auto negotiation can be read from the SGMII Management Auto negotiation Link Partner Ability Base Register (Table 131). The duplex mode and speed of the XPS_LL_TEMAC should then be set to match (see "TEMAC Receive Configuration Word 1 (RCW1) Registers" on page 56, "TEMAC Transmit Configuration (TC) Registers" on page 58, and "TEMAC Ethernet MAC Mode Configuration (EMMC) Registers" on page 60).

There are two methods that may be used to learn of the completion of an auto negotiation cycle:

- By polling the auto negotiation complete bit of SGMII Management Status Register (Register 1, bit 5 Table 127).
- By using the auto negotiation complete interrupt (See "Interrupt Status Registers (IS0 and IS1)" on page 32 and SGMII Management Auto Negotiation Interrupt Control Register Table 136 on page 146.)

Loopback

There are two possible loopback positions:

- **Loopback in the Hard TEMAC silicon component**. When placed into loopback, data is routed from the transmitter to the receiver path at the last possible point in the PCS/PMA sublayer. This is immediately before the RocketIO transceiver interface. When placed into loopback, a constant stream of Idle code groups is transmitted through the RocketIO transceiver. Loopback in this position allows test frames to be looped back within the system without allowing them to be received by the link partner (the device connected on the other end of the Ethernet. The transmission of Idles allows the link partner to remain in synchronization so that no fault is reported.
- **Loopback in the RocketIO transceiver**. The RocketIO can be switched into loopback and will route data from the transmitter path to the receiver path within the RocketIO transceiver. However, this data is also transmitted out of the RocketIO transceiver and so any test frames used for a loopback test will be received by the link partner.

Loopback can be enabled or disabled by writing to the SGMII Management Control Register bit 14 (Table 126 on page 142) while the loopback position can be controlled by writing the SGMII Management Loopback Control Register bit 0 (Table 137 on page 146).

1000BASE-X PCS/PMA

Please refer to the UG074 *Virtex-4 FPGA Embedded Tri-Mode Ethernet MAC User Guide v1.9* for an equivalent diagram of the clock management scheme.

PCS/PMA

The Physical Coding Sublayer (PCS) for 1000BASE-X operation is defined in IEEE 802.3 clause 36 and 37 and performs the following:

- Encoding (and decoding) of GMII data octets to form a sequence of ordered sets
- 8B/10B encoding (and decoding) of the sequence ordered sets
- 1000BASE-X Auto-Negotiation for information exchange with the link partner

The Physical Medium Attachment (PMA) for 1000BASE-X operation is defined in IEEE 802.3 clause 36 and performs the following:

- Serialization (and de serialization) of code-groups for transmission (and reception) on the underlying serial PMD
- recovery of clock from the 8B/10B coded data supplied by the PMD

1000BASE-X PCS/PMA functionality is provided by connecting the Hard TEMAC silicon component to a RocketIO transceiver.

PMD

The Physical Medium Dependent (PMD) sublayer is defined in IEEE 802.3 clause 38 for 1000BASE-LX and 1000BASE-SX (long and short wave laser). This type of PMD is provided by the external GBIC or SFP optical transceiver which should be connected directly to the ports of the RocketIO transceiver.

Virtex 4 Hard TEMAC 1000BASE-X Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

1000BASE-X Auto-Negotiation

1000BASE-X auto negotiation is described in IEEE Std 802.3, clause 37. This function allows a device to advertise the supported modes of operation to a device at the remote end of a link segment (the link partner on Ethernet), and detect corresponding operational modes advertised by the link partner.

The results of the auto negotiation can be read from the 1000BASE-X Management Auto negotiation Link Partner Ability Base Register (Table 118). The duplex mode and speed of the XPS_LL_TEMAC should then be set to match (see "TEMAC Receive Configuration Word 1 (RCW1) Registers" on page 56, "TEMAC Transmit Configuration (TC) Registers" on page 58, and "TEMAC Ethernet MAC Mode Configuration (EMMC) Registers" on page 60).

There are two methods that may be used to learn of the completion of an auto negotiation cycle:

- By polling the auto negotiation complete bit of 1000BASE-X Management Status Register (Register 1, bit 5 Table 114).

By using the auto negotiation complete interrupt (See "Interrupt Status Registers (IS0 and IS1)" on page 32 and 1000BASE-X Management Auto Negotiation Interrupt Control Register Table 123 on page 140.)

Loopback

There are two possible loopback positions:

- **Loopback in the Hard TEMAC silicon component**. When placed into loopback, data is routed from the transmitter to the receiver path at the last possible point in the PCS/PMA sublayer. This is immediately before the RocketIO transceiver interface. When placed into loopback, a constant stream of Idle code groups is transmitted through the RocketIO transceiver. Loopback in this position allows test frames to be looped back within the system without allowing them to be received by the link partner (the device connected on the other end of the Ethernet. The transmission of Idles allows the link partner to remain in synchronization so that no fault is reported.
- **Loopback in the RocketIO transceiver**. The RocketIO transceiver can be switched into loopback and will route data from the transmitter path to the receiver path within the RocketIO transceiver. However, this data is also transmitted out of the RocketIO transceiver and so any test frames used for a loopback test will be received by the link partner.

Loopback can be enabled or disabled by writing to the 1000BASE-X Management Control Register bit 14 (Table 124 on page 141) while the loopback position can be controlled by writing the 1000BASE-X Management Loopback Control Register bit 0 (Table 98 on page 125).

Internal 1000BASE-X PCS/PMA Management Registers

Registers 0 through 15 are defined in IEEE 802.3. These registers contain information relating to the operation of the 1000BASE-X PCS/PMA sublayer, including the status of the physical Ethernet link (PHY Link).

Additionally, these registers are directly involved in the operation of the 1000BASE-X auto negotiation function which occurs between the XPS_LL_TEMAC and its link partner, the Ethernet device connected at the far end of the PHY Link.

These registers are accessed via the MII Management interface (See "Using the MII Management to Access Internal or External PHY Registers" on page 73). These registers are only valid when using the 1000BASE-X PHY interface.

When using 1000BASE-X, the XPS_LL_TEMAC is typically connected to an external optical transceiver device such as a GBIC or SFP transceiver.

Table 112: **Internal 1000BASE-X PCS/PMA Management Registers**

Register Name	Register Address (REGAD)
Control Register (Register 0)	0
Status Register (Register 1)	1
PHY Identifier (Register 2 and 3)	2,3
Auto Negotiation Advertisement Register (Register 4)	4
Auto Negotiation Link Partner Ability Base Register (Register 5)	5
Auto Negotiation Expansion Register (Register 6)	6
Auto Negotiation Next Page Transmit Register (Register 7)	7
Auto Negotiation Next Page Receive Register (Register 8)	8
Extended Status Register (Register 15)	15
Vendor Specific Register: Auto Negotiation Interrupt Control Register (Register 16)	16
Vendor Specific Register: Loopback Control Register (Register 17)	17

Table 113 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Control Register bit definitions.

Table 113: **1000BASE-X Management Control Register (Register 0) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Reset	Read/Write self clearing	0	0 - normal operation 1 - PCS/PMA reset
14	Loopback	Read/Write	0	0 - disable loopback mode 1 - enable loopback mode
13	Speed Selection (LSB)	Returns 0	0	Always returns 0 for this bit. Along with bit 6, speed selection of 1000 Mb/S is identified.
12	Auto Negotiation Enable	Read/Write	1	0 - disable auto negotiation 1 - enable auto negotiation

Table 113: **1000BASE-X Management Control Register (Register 0) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
11	Power Down	Read/Write	0	When set to "1", the RocketIO MGT is placed in a low power state. This bit requires a reset (bit 15) to clear. 0 - normal operation 1 - power down
10	Isolate	Read/Write	0	0 - normal operation 1 - electrically isolate the PHY
9	Restart Auto Negotiation	Read/Write self clearing	0	0 - normal operation 1 - restart auto negotiation process
8	Duplex Mode	Returns 1	1	Always returns 1 for this bit to disable COL test.
7	Collision Test	Returns 0	0	Always returns 0 for this bit to signal full duplex mode.
6	Speed Selection (MSB)	Returns 1	1	Always returns 1 for this bit. Along with bit 13, speed selection of 1000 Mb/S is identified.
5	Unidirectional Enable	Read/Write	0	Enable transmit regardless of whether a valid link has been established.
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 114 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Status Register bit definitions.

Table 114: **1000BASE-X Management Status Register (Register 1) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	100BASE-T4	Returns 0	0	Always returns a 0 for this bit because 100BASE-T4 is not supported.
14	100BASE-X Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X full duplex is not supported.
13	100BASE-X Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X half duplex is not supported.
12	10 Mb/S Full Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S full duplex is not supported.
11	10 Mb/S Half Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S half duplex is not supported.
10	100BASE-T2 Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 full duplex is not supported.
9	100BASE-T2 Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 half duplex is not supported.
8	Extended Status	Returns 1	1	Always returns a 1 for this bit indicating the presence of the extended register (register 15).
7	Unidirectional Ability	Returns 1	1	Always returns a 1.
6	MF Preamble Suppression	Returns 1	1	Always returns a 1 for this bit to indicate the support of management frame preamble suppression.

Table 114: **1000BASE-X Management Status Register (Register 1) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
5	Auto Negotiation Complete	Read	0	0 - auto negotiation process not completed 1 - auto negotiation process complete
4	Remote Fault	Read only self clearing on read	0	0 - no remote fault condition detected 1 - remote fault condition detected
3	Auto Negotiation Ability	Returns 1	1	Always returns a q for this bit indicating that the PHY is capable of auto negotiation.
2	Link Status	Read only self clearing on read	0	0 - PHY Link is down 1 - PHY Link is up
1	Jabber Detect	Returns 0	0	Always returns a 0 for this bit because no jabber detect is supported.
0	Extended Capability	Returns 0	0	Always returns a 0 for this bit because no extended register set is supported.

Table 115 shows the first Hard TEMAC Internal 1000BASE-X PCS/PMA Management PHY Identifier Register bit definitions.

Table 115: **1000BASE-X Management PHY Identifier (Register 2) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	OUI	Read	returns OUI (3-18) 0x0028	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.

Table 116 shows the second Hard TEMAC Internal 1000BASE-X PCS/PMA Management PHY Identifier Register bit definitions.

Table 116: **1000BASE-X Management PHY Identifier (Register 3) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
10 - 15	OUI	Read	returns OUI (19-24) 0x0035	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.
30	MMN	Returns 0	0	Manufacturer's Model Number. Always returns 0s.
29	Revision	Returns 0	0	Revision Number. Always returns 0s.

Table 117 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Advertisement Register bit definitions.

Table 117: **1000BASE-X Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/Write	0	0 - next page functionality is not advertised 1 - next page functionality is advertised
14	Reserved	Returns 0s	0	Always return zeros.

Table 117: **1000BASE-X Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
12 - 13	Remote Fault	Read/Write self clearing after auto negotiation	0x0	00 - no error 01 - offline 10 - link failure 11 - auto negotiation error
9 - 11	Reserved	Returns 0s	0x0	Always return zeros.
7 - 8	Pause	Read/write	0x3	00 - no pause 01 - asymmetric pause towards link partner 10 - symmetric pause 11 - both symmetric pause and asymmetric pause towards link partner
6	Half Duplex	Returns 0	0	Always return zeros because half duplex is not supported.
5	Full Duplex	Read/Write	1	0 - full duplex mode is not advertised 1 - full duplex mode is advertised
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 118 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto negotiation Link Partner Ability Base Register bit definitions.

Table 118: **1000BASE-X Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - next page functionality is not supported 1 - next page functionality is supported
14	Acknowledge	Read	0	Used by the auto negotiation function to indicate reception of a link partner's base or next page.
12 - 13	Remote Fault	Read/	0x0	00 - no error 01 - offline 10 - link failure 11 - auto negotiation error
9 - 11	Reserved	Returns 0s	0x0	Always return zeros.
7 - 8	Pause	Read	0x0	00 - no pause 01 - asymmetric pause supported 10 - symmetric pause supported 11 - both symmetric pause and asymmetric pause supported
6	Half Duplex	Read	0	0 - half duplex mode is not supported 1 - half duplex mode is supported
5	Full Duplex	Read/	0	0 - full duplex mode is not supported 1 - full duplex mode is supported
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 119 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto negotiation Expansion Register bit definitions.

Table 119: **1000BASE-X Management Auto Negotiation Expansion Register (Register 6) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
3 - 15	Reserved	Returns 0s	0x0	Always return zeros.
2	Next Page Able	Returns 1	1	Always returns a 1 for this bit because the device is Next Page Able.
1	Page Received	Read self clearing on read	0	0 - a new page is not received 1 - a new page is received
0	Reserved	Returns 0s	0	Always return zeros.

Table 120 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Next Page Transmit Register bit definitions.

Table 120: **1000BASE-X Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/Write	0	0 - last page 1 - additional next page(s) will follow
14	Reserved	Returns 0s	0	Always return zeros.
13	Message Page	Read/Write	1	0 - unformatted page 1 - message page
12	Acknowledge 2	Read/Write	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read/Write	0x001 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 121 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Next Page Receive Register bit definitions.

Table 121: **1000BASE-X Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - last page 1 - additional next page(s) will follow
14	Acknowledge	Read	0	Used by auto negotiation function to indicate reception of a link partner's base or next page.
13	Message Page	Read	0	0 - unformatted page 1 - message page

Table 121: **1000BASE-X Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
12	Acknowledge 2	Read	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read	0x0 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 122 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Extended Status Register bit definitions.

Table 122: **1000BASE-X Management Extended Status Register (Register 15) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	1000BASE-X Full Duplex	Returns 1	1	Always returns a 1 for this bit because 1000BASE-X full duplex is supported.
14	1000BASE-X Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-X half duplex is not supported.
13	1000BASE-T Full Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T full duplex is not supported.
12	1000BASE-T Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T half duplex is not supported.
0 - 11	Reserved	Returns 0s	0x0	Always return zeros.

Table 123 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Auto Negotiation Interrupt Control Register bit definitions.

Table 123: **1000BASE-X Management Auto Negotiation Interrupt Control Register (Register 16) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
2 - 15	Reserved	Returns 0s	0	Always return zeros.
1	Interrupt Status	Read/Write	0	If the interrupt is enabled, this bit will be asserted upon the completion of an auto negotiation cycle; it will only be cleared by writing 0 to this bit. If the interrupt is disabled, this bit will be set to 0. This is the auto negotiation complete interrupt. 0 - interrupt is asserted 1 - interrupt is not asserted
0	Interrupt Enable	Read/Write	1	0 - interrupt is disabled 1 - interrupt is enabled

Table 124 shows the Hard TEMAC Internal 1000BASE-X PCS/PMA Management Loopback Control Register bit definitions.

Table 124: **1000BASE-X Management Loopback Control Register (Register 17) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
1 - 15	Reserved	Returns 0s	0	Always return zeros.
0	Loopback Position	Read/Write	0	Loopback is enabled or disabled using register 0 bit 14. 0 - loopback (when enabled) occurs directly before the interface to the RocketIO transceiver 1 - loopback (when enabled) occurs in the RocketIO transceiver

Internal SGMII Management Registers

Registers 0 through 15 are defined in IEEE 802.3. These registers contain information relating to the operation of the SGMII PCS sublayer, including the status of both the SGMII Link and the physical Ethernet link (PHY Link).

Additionally, these registers are directly involved in the operation of the SGMII auto negotiation function which occurs between the XPS_LL_TEMAC and the external PHY device (typically a tri-speed BASE-T PHY).

These registers are accessed via the MII Management interface (See "Using the MII Management to Access Internal or External PHY Registers" on page 73). These registers are only valid when using the SGMII PHY interface.

Table 125: **Internal SGMII Management Registers**

Register Name	Register Address (REGAD)
SGMII Control Register (Register 0)	0
SGMII Status Register (Register 1)	1
SGMII PHY Identifier (Register 2 and 3)	2,3
SGMII Auto Negotiation Advertisement Register (Register 4)	4
SGMII Auto Negotiation Link Partner Ability Base Register (Register 5)	5
SGMII Auto Negotiation Expansion Register (Register 6)	6
SGMII Auto Negotiation Next Page Transmit Register (Register 7)	7
SGMII Auto Negotiation Next Page Receive Register (Register 8)	8
SGMII Extended Status Register (Register 15)	15
SGMII Vendor Specific Register: Auto Negotiation Interrupt Control Register (Register 16)	16
SGMII Vendor Specific Register: Loopback Control Register (Register 17)	17

Table 126 shows the Hard TEMAC Internal SGMII PCS Management Control Register bit definitions.

Table 126: **SGMII Management Control Register (Register 0) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Reset	Read/Write self clearing	0	0 - normal operation 1 - PCS/PMA reset
14	Loopback	Read/Write	0	0 - disable loopback mode 1 - enable loopback mode
13	Speed Selection (LSB)	Returns 0	0	Always returns 0 for this bit. Along with bit 6, speed selection of 1000 Mb/S is identified.
12	Auto Negotiation Enable	Read/Write	1	0 - disable auto negotiation 1 - enable auto negotiation
11	Power Down	Read/Write	0	When set to "1", the RocketIO MGT is placed in a low power state. This bit requires a reset (bit 15) to clear. 0 - normal operation 1 - power down
10	Isolate	Read/Write	0	0 - normal operation 1 - electrically isolate the PHY
9	Restart Auto Negotiation	Read/Write self clearing	0	0 - normal operation 1 - restart auto negotiation process
8	Duplex Mode	Returns 1	1	Always returns 1 for this bit to disable COL test.
7	Collision Test	Returns 0	0	Always returns 0 for this bit to signal full duplex mode.
6	Speed Selection (MSB)	Returns 1	1	Always returns 1 for this bit. Along with bit 13, speed selection of 1000 Mb/S is identified.
5	Unidirectional Enable	Read/Write	0	Enable transmit regardless of whether a valid link has been established.
0 - 4	Reserved	Returns 0s	0x0	Always return zeros.

Table 127 shows the Hard TEMAC Internal SGMII PCS Management Status Register bit definitions.

Table 127: **SGMII Management Status Register (Register 1) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	100BASE-T4	Returns 0	0	Always returns a 0 for this bit because 100BASE-T4 is not supported.
14	100BASE-X Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X full duplex is not supported.
13	100BASE-X Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-X half duplex is not supported.
12	10 Mb/S Full Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S full duplex is not supported.
11	10 Mb/S Half Duplex	Returns 0	0	Always returns a 0 for this bit because 10 Mb/S half duplex is not supported.

Table 127: **SGMII Management Status Register (Register 1) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
10	100BASE-T2 Full Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 full duplex is not supported.
9	100BASE-T2 Half Duplex	Returns 0	0	Always returns a 0 for this bit because 100BASE-T2 half duplex is not supported.
8	Extended Status	Returns 1	1	Always returns a 1 for this bit indicating the presence of the extended register (register 15).
7	Unidirectional Ability	Returns 1	1	Always returns a 1.
6	MF Preamble Suppression	Returns 1	1	Always returns a 1 for this bit to indicate the support of management frame preamble suppression.
5	Auto Negotiation Complete	Read	0	0 - auto negotiation process not completed 1 - auto negotiation process complete
4	Remote Fault	Read only self clearing on read	0	0 - no remote fault condition detected 1 - remote fault condition detected
3	Auto Negotiation Ability	Returns 1	1	Always returns a q for this bit indicating that the PHY is capable of auto negotiation.
2	Link Status	Read only self clearing on read	0	0 - PHY Link is down 1 - PHY Link is up
1	Jabber Detect	Returns 0	0	Always returns a 0 for this bit because no jabber detect is supported.
0	Extended Capability	Returns 0	0	Always returns a 0 for this bit because no extended register set is supported.

Table 128 shows the first Hard TEMAC Internal SGMII PCS Management PHY Identifier Register bit definitions.

Table 128: **SGMII Management PHY Identifier (Register 2) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	OUI	Read	returns OUI (3-18) 0x0028	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.

Table 129 shows the second Hard TEMAC Internal SGMII PCS Management PHY Identifier Register bit definitions.

Table 129: **SGMII Management PHY Identifier (Register 3) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
10 - 15	OUI	Read	returns OUI (19-24) 0x0035	Organizationally Unique Identifier (OUI) from IEEE is 0x000A35.
30	MMN	Returns 0	0	Manufacturer's Model Number. Always returns 0s.
29	Revision	Returns 0	0	Revision Number. Always returns 0s.

Table 130 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Advertisement Register bit definitions.

Table 130: **SGMII Management Auto Negotiation Advertisement Register (Register 4) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 15	All bits	Read	0x0001	SGMII defined value sent from the MAC to the PHY.

Table 131 shows the Hard TEMAC Internal SGMII PCS Management Auto negotiation Link Partner Ability Base Register bit definitions.

Table 131: **SGMII Management Auto negotiation Link Partner Ability Base Register (Register 5) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	PHY Link Status	Read	1	This refers to the link status of the external PHY device with its Link Partner across the PHY Link. 0 - link down 1 - link up
14	Acknowledge	Read	0	Used by the auto negotiation function to indicate reception of a link partner's base or next page.
13	Reserved	Returns 0	0	Always return zero.
12	Duplex Mode	Read	0	The resolved duplex mode that the external PHY device has auto negotiated with its Link Partner across the PHY Link. 0 - half duplex 1 - full duplex
10 - 11	Speed	Read	0x0	The resolved operating speed that the external PHY device has auto negotiated with its Link Partner across the PHY Link. 00 - 10 Mb/S 01 - 100 Mb/S 10 -1000 Mb/S 11 - Reserved
1 - 9	Reserved	Returns 0s	0x0	Always return zeros.
0	Reserved	Returns 1	1	Always return one.

Table 132 shows the Hard TEMAC Internal SGMII PCS Management Auto negotiation Expansion Register bit definitions.

Table 132: **SGMII Management Auto Negotiation Expansion Register (Register 6) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
3 - 15	Reserved	Returns 0s	0x0	Always return zeros.
2	Next Page Able	Returns 1	1	Always returns a 1 for this bit because the device is Next Page Able.

Table 132: **SGMII Management Auto Negotiation Expansion Register (Register 6) Bit Definitions *(Cont'd)***

Bit(s)	Name	Core Access	Reset Value	Description
1	Page Received	Read self clearing on read	0	0 - a new page is not received 1 - a new page is received
0	Reserved	Returns 0s	0	Always return zeros.

Table 133 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Next Page Transmit Register bit definitions.

Table 133: **SGMII Management Auto Negotiation Next Page Transmit Register (Register 7) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read/write	0	0 - last page 1 - additional next page(s) will follow
14	Reserved	Returns 0s	0	Always return zeros.
13	Message Page	Read/Write	1	0 - unformatted page 1 - message page
12	Acknowledge 2	Read/Write	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read/Write	0x001 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 134 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Next Page Receive Register bit definitions.

Table 134: **SGMII Management Auto Negotiation Next Page Receive Register (Register 8) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	Next Page	Read	0	0 - last page 1 - additional next page(s) will follow
14	Acknowledge	Read	0	Used by auto negotiation function to indicate reception of a link partner's base or next page.
13	Message Page	Read	0	0 - unformatted page 1 - message page
12	Acknowledge 2	Read	0	0 - cannot comply with message 1 - complies with message
11	Toggle	Read	0	Value toggles between sequent pages.
0 -10	Message or unformatted Code Field	Read	0x0 (null message code)	Message code field or unformatted page encoding as dictated by bit 13.

Table 135 shows the Hard TEMAC Internal SGMII PCS Management Extended Status Register bit definitions.

Table 135: **SGMII Management Extended Status Register (Register 15) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
15	1000BASE-X Full Duplex	Returns 1	1	Always returns a 1 for this bit because 1000BASE-X full duplex is supported.
14	1000BASE-X Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-X half duplex is not supported.
13	1000BASE-T Full Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T full duplex is not supported.
12	1000BASE-T Half Duplex	Returns 0	0	Always returns a 1 for this bit because 1000BASE-T half duplex is not supported.
0 - 11	Reserved	Returns 0s	0x0	Always return zeros.

Table 136 shows the Hard TEMAC Internal SGMII PCS Management Auto Negotiation Interrupt Control Register bit definitions.

Table 136: **SGMII Management Auto Negotiation Interrupt Control Register (Register 16) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
2 - 15	Reserved	Returns 0s	0	Always return zeros.
1	Interrupt Status	Read/Write	0	If the interrupt is enabled, this bit will be asserted upon the completion of an auto negotiation cycle; it will only be cleared by writing 0 to this bit. If the interrupt is disabled, this bit will be set to 0. This is the auto negotiation complete interrupt. 0 - interrupt is asserted 1 - interrupt is not asserted
0	Interrupt Enable	Read/Write	1	0 - interrupt is disabled 1 - interrupt is enabled

Table 137 shows the Hard TEMAC Internal SGMII PCS Management Loopback Control Register bit definitions.

Table 137: **SGMII Management Loopback Control Register (Register 17) Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
1 - 15	Reserved	Returns 0s	0	Always return zeros.
0	Loopback Position	Read/Write	0	Loopback is enabled or disabled using register 0 bit 14. 0 - loopback (when enabled) occurs directly before the interface to the RocketIO transceiver 1 - loopback (when enabled) occurs in the RocketIO transceiver

Soft TEMAC Implementations

Introduction to Physical Interfaces

The soft TEMAC implementation is independent of, and can connect to, any type of physical layer device. The XPS_LL_TEMAC provides additional circuitry around the soft TEMAC to allow easy use of two of the most common physical layer device interfaces.

Because the soft TEMAC uses more logic and clock resources than a Hard TEMAC implementation, it is less likely that multiple channels will be used in one device.

Please refer to Table 1 on page 4 for supported voltages with the different device families.

Media Independent Interface (MII)

The Media Independent Interface (MII), defined in IEEE 802.3 clause 22, is a parallel interface that connects at 10-Mb/S and/or 100-Mb/S to external PHY devices.

Please refer toUG138 LogicCORE IP Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme.

Soft TEMAC MII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

Gigabit Media Independent Interface (GMII)

The Gigabit Media Independent Interface (GMII), defined in IEEE 802.3 clause 35, is an extension of the MII used to connect at 1-Gb/S to the PHY devices.

MII can be considered a subset of GMII, and as a result, GMII/MII together can carry Ethernet traffic at 10 Mb/S, 100 Mb/S, and 1 Gb/S.

When the GMII interface is selected with parameters for the XPS_LL_TEMAC, a GMII/MII interface is used which is capable of all three Ethernet speeds.

Please refer toUG138 LogicCORE IP Tri-Mode Ethernet MAC User Guide for an equivalent diagram of the clock management scheme.

Soft TEMAC GMII Constraints

Refer to Answer Record 32713 for constraint examples. Refer to UG625 for an overview of the various constraints used.

Design Implementation

Target Technology

The intended target technology are Spartan-3E, Spartan-3A, Spartan-3AN, Spartan-3ADSP, Spartan 6, Virtex-4, Virtex-5, and Virtex-6 FPGAs.

Device Utilization and Performance Benchmarks

Because the XPS_LL_TEMAC is a module that will be used with other design pieces in the FPGA, the utilization and timing numbers reported in this section are just estimates. As the XPS_LL_TEMAC is

combined with other pieces of the FPGA design, the utilization of the FPGA resources and the timing of the XPS_LL_TEMAC design will vary from the results reported here. The XPS_LL_TEMAC benchmarks for GMII systems are shown in Table 138 for a Virtex-6 FPGA, in Table 139 for a Virtex-5 FPGA, in Table 140 for a Virtex-4 FPGA, in Table 141 for a Spartan-6 FPGA, and in Table 142 for a Spartan-3 FPGA.

Table 138: **XPS_LL_TEMAC Virtex-6 FPGA Performance and Resource Utilization Benchmarks**

Parameter Values								Device Resources				
C_TEMAC1_ENABLED	C_TEMAC(0,1)_(T,R)XFIFO	C_TEMAC(0,1)_(T,R)XCSUM	C_TEMAC(0,1)_TXVLAN_*	C_TEMAC(0,1)_RXVLAN_*	C_TEMAC(0,1)_MCAST_EXTEND	C_TEMAC(0,1)_STATS	C_TEMAC_TYPE	Slices	Flip- Flops	BRAMS	6-input LUTs	BUFGs
0	2048	0	0	0	0	0	2	1160	2661	4	3079	2
0	2048	0	0	0	0	0	0	644	1538	4	1679	5
0	16384	0	0	0	0	0	2	1181	2733	10	3246	2
1	16384	0	0	0	0	0	2	2129	5110	20	6179	3
1	16384	1	0	0	0	0	2	2503	5694	20	7061	3
0	16384	1	0	0	0	0	2	1336	3025	10	3678	2
0	32768	0	0	0	0	0	2	1242	2760	18	3385	2
1	32768	0	0	0	0	0	2	2149	5163	36	6482	3
1	32768	1	0	0	0	0	2	2713	5747	36	7373	3
0	32768	1	0	0	0	0	2	1307	3052	18	3801	2
0	16384	0	0	0	0	0	0	706	1610	10	1870	5
1	16384	0	0	0	0	0	0	1543	2997	20	3586	9
1	16384	1	0	0	0	0	0	1638	3581	20	4450	9
0	16384	1	0	0	0	0	0	844	1902	10	2290	5
0	32768	0	0	0	0	0	0	726	1637	18	2006	5
1	32768	0	0	0	0	0	0	1430	3051	36	3877	9
1	32768	1	0	0	0	0	0	1617	3635	36	4726	9
0	32768	1	0	0	0	0	0	863	1929	18	2428	5
0	32768	1	0	0	0	1	0	1152	2835	18	3339	6
0	32768	1	0	0	1	1	0	1174	2924	19	3445	6
0	32768	0	0	1	1	1	0	1378	3102	21	3688	6
0	32768	0	1	1	1	1	0	1277	3104	23	3677	6
1	32768	0	1	1	1	1	0	2533	5970	46	7206	10

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Table 139: **XPS_LL_TEMAC Virtex-5 FPGA Performance and Resource Utilization Benchmarks**

Parameter Values								Device Resources				
C_TEMAC1_ENABLED	C_TEMAC(0,1)_(T,R)XFIFO	C_TEMAC(0,1)_(T,R)XCSUM	C_TEMAC(0,1)_TXVLAN_*	C_TEMAC(0,1)_RXVLAN_*	C_TEMAC(0,1)_MCAST_EXTEND	C_TEMAC(0,1)_STATS	C_TEMAC_TYPE	Slices	Flip- Flops	BRAMS	4-input LUTs	BUFGs
0	2048	0	0	0	0	0	2	1544	2670	3	2634	3
0	2048	0	0	0	0	0	0	845	1498	3	1373	6
0	16384	0	0	0	0	0	2	1656	2741	18	2870	3
1	16384	0	0	0	0	0	2	2898	5123	36	5656	5
1	16384	1	0	0	0	0	2	3105	5709	36	6337	5
0	16384	1	0	0	0	0	2	1802	3033	18	3213	3
0	32768	0	0	0	0	0	2	1616	2767	34	2921	3
1	32768	0	0	0	0	0	2	2981	5176	68	5741	5
1	32768	1	0	0	0	0	2	3326	5762	68	6416	5
0	32768	1	0	0	0	0	2	1836	3060	34	3263	3
0	16384	0	0	0	0	0	0	880	1573	18	1570	6
1	16384	0	0	0	0	0	0	1719	2918	36	3093	10
1	16384	1	0	0	0	0	0	1952	3504	36	3754	10
0	16384	1	0	0	0	0	0	1018	1866	18	1898	6
0	32768	0	0	0	0	0	0	913	1600	34	1620	6
1	32768	0	0	0	0	0	0	1785	2972	68	3197	10
1	32768	1	0	0	0	0	0	2076	3558	68	3858	10
0	32768	1	0	0	0	0	0	1012	1893	34	1952	6
0	32768	1	0	0	0	1	0	1452	2797	34	2793	7
0	32768	1	0	0	1	1	0	1556	2888	36	2908	7
0	32768	0	0	1	1	1	0	1728	3071	40	3052	7
0	32768	0	1	1	1	1	0	1609	3073	44	3066	7
1	32768	0	1	1	1	1	0	3338	5907	88	6059	11

Table 140: **XPS_LL_TEMAC Virtex-4 FPGA Performance and Resource Utilization Benchmarks**

Parameter Values								Device Resources				
C_TEMAC1_ENABLED	C_TEMAC(0,1)_(T,R)XFIFO	C_TEMAC(0,1)_(T,R)XCSUM	C_TEMAC(0,1)_TXVLAN_*	C_TEMAC(0,1)_RXVLAN_*	C_TEMAC(0,1)_MCAST_EXTEND	C_TEMAC(0,1)_STATS	C_TEMAC_TYPE	Slices	Flip- Flops	BRAMS	4-input LUTs	BUFGMUXs
0	2048	0	0	0	0	0	2	2671	2714	4	3506	2
0	2048	0	0	0	0	0	1	1623	1647	4	2060	6
0	16384	0	0	0	0	0	2	2767	2789	18	3710	2
1	16384	0	0	0	0	0	2	5291	5222	36	7225	3
1	16384	1	0	0	0	0	2	5819	5810	36	7987	3
0	16384	1	0	0	0	0	2	3017	3080	18	4106	2
0	32768	0	0	0	0	0	2	2855	2816	34	3889	2
1	32768	0	0	0	0	0	2	5446	5275	68	7480	3
1	32768	1	0	0	0	0	2	5982	5861	68	8285	3
0	32768	1	0	0	0	0	2	3124	3107	34	4286	2
0	16384	0	0	0	0	0	1	1708	1720	18	2254	6
1	16384	0	0	0	0	0	1	3136	3103	36	4217	10
1	16384	1	0	0	0	0	1	3649	3687	36	4974	10
0	16384	1	0	0	0	0	1	1952	2012	18	2642	6
0	32768	0	0	0	0	0	1	1789	1746	34	2418	6
1	32768	0	0	0	0	0	1	3310	3155	68	4546	10
1	32768	1	0	0	0	0	1	3833	3741	68	5343	10
0	32768	1	0	0	0	0	1	2044	2039	34	2811	6
0	32768	1	0	0	0	1	1	2913	2978	36	3461	7
0	32768	1	0	0	1	1	1	2996	3069	38	3560	7
0	32768	0	0	1	1	1	1	3276	3252	42	3846	7
0	32768	0	1	1	1	1	1	3276	3254	46	3856	7
1	32768	0	1	1	1	1	1	6266	6154	92	7643	11

Table 141: **XPS_LL_TEMAC Spartan-6 FPGA Performance and Resource Utilization Benchmarks**

Parameter Values								Device Resources				
C_TEMAC1_ENABLED	C_TEMAC(0,1)_(T,R)XFIFO	C_TEMAC(0,1)_(T,R)XCSUM	C_TEMAC(0,1)_TXVLAN_*	C_TEMAC(0,1)_RXVLAN_*	C_TEMAC(0,1)_MCAST_EXTEND	C_TEMAC(0,1)_STATS	C_TEMAC_TYPE	Slices	Flip- Flops	BRAMS	6-input LUTs	BUFGs
0	2048	0	0	0	0	0	2	1136	2660	4	3175	2
0	16384	0	0	0	0	0	2	1318	2735	18	3369	2
1	16384	0	0	0	0	0	2	2413	5114	36	6432	4
1	16384	1	0	0	0	0	2	2689	5697	36	7407	4
0	16384	1	0	0	0	0	2	1438	3027	18	3822	2
0	32768	0	0	0	0	0	2	1284	2762	34	3438	2
1	32768	0	0	0	0	0	2	2421	5167	68	6645	4
1	32768	1	0	0	0	0	2	2736	5751	68	7514	4
0	32768	1	0	0	0	0	2	1468	3054	34	3870	2
0	32768	1	0	0	0	1	2	1845	4026	34	4825	2
0	32768	1	0	0	1	1	2	1871	4120	36	4948	2
0	32768	0	0	1	1	1	2	2073	4299	40	5236	2
0	32768	0	1	1	1	1	2	1994	4301	44	5228	2
1	32768	0	1	1	1	1	2	3895	8230	88	10154	4

Table 142: **XPS_LL_TEMAC Spartan-3 FPGA Performance and Resource Utilization Benchmarks**

Parameter Values								Device Resources				
C_TEMAC1_ENABLED	C_TEMAC(0,1)_(T,R)XFIFO	C_TEMAC(0,1)_(T,R)XCSUM	C_TEMAC(0,1)_TXVLAN_*	C_TEMAC(0,1)_RXVLAN_*	C_TEMAC(0,1)_MCAST_EXTEND	C_TEMAC(0,1)_STATS	C_TEMAC_TYPE	Slices	Flip- Flops	BRAMS	4-input LUTs	BUFGMUXs
0	2048	0	0	0	0	0	2	2666	2707	4	3489	4
0	16384	0	0	0	0	0	2	2746	2780	18	3682	4
1	16384	0	0	0	0	0	2	5232	5196	36	7132	7
1	16384	1	0	0	0	0	2	5749	5784	36	7887	7
0	16384	1	0	0	0	0	2	2988	3071	18	4051	4
0	32768	0	0	0	0	0	2	2822	2804	34	3831	4
1	32768	0	0	0	0	0	2	5400	5250	68	7449	7
1	32768	1	0	0	0	0	2	5918	5842	68	8207	7
0	32768	1	0	0	0	0	2	3080	3098	34	4210	4
0	32768	1	0	0	0	1	2	3991	4104	36	4958	5
0	32768	1	0	0	1	1	2	4090	4198	38	5112	5
0	32768	0	0	1	1	1	2	4336	4376	42	5368	5
0	32768	0	1	1	1	1	2	4344	4378	46	5378	5
1	32768	0	1	1	1	1	2	8410	8399	92	10476	8

System Performance

To measure the system performance (F_{MAX}) of the XPS LL TEMAC core, it core was added to a Virtex-6 FPGA system, a Virtex-5 FPGA system, a Virtex-4 FPGA system, a Spartan-6 FPGA system, and a Spartan-3A DSP FPGA system as the Device Under Test (DUT) as shown in Figure 60, Figure 61, Figure 62, Figure 63, and Figure 64.

Because the XPS LL TEMAC core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When this core is combined with other designs in the system, the utilization of FPGA resources and timing of the core design will vary from the results reported here.

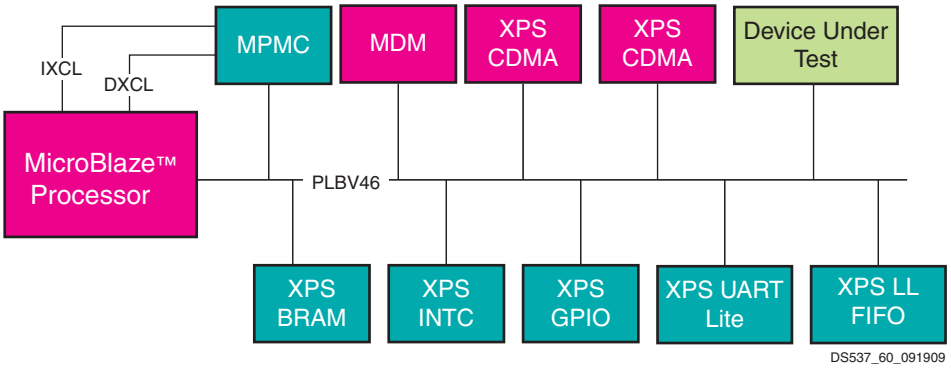

Figure 60: **Virtex-6 FPGA System with the XPS LL TEMAC as the DUT**

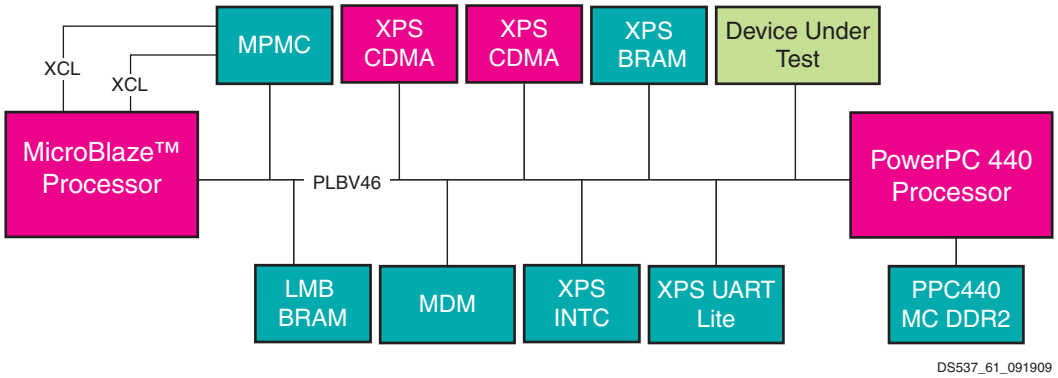

Figure 61: **Virtex-5 FPGA System with the XPS LL TEMAC as the DUT**

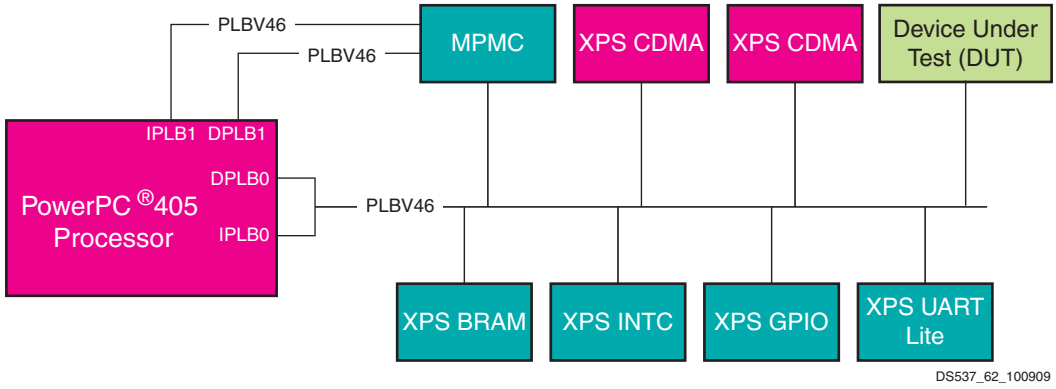

Figure 62: **Virtex-4 FPGA System with the XPS LL TEMAC as the DUT**

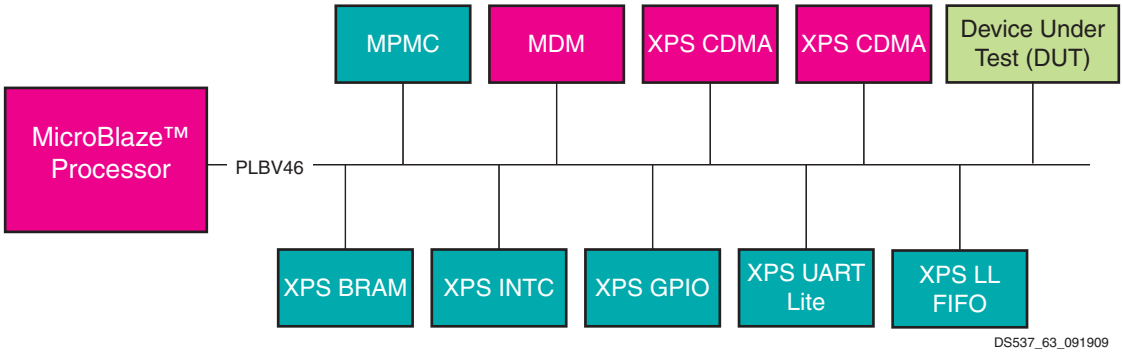

Figure 63: **Spartan-6 FPGA System with the XPS LL TEMAC as the DUT**

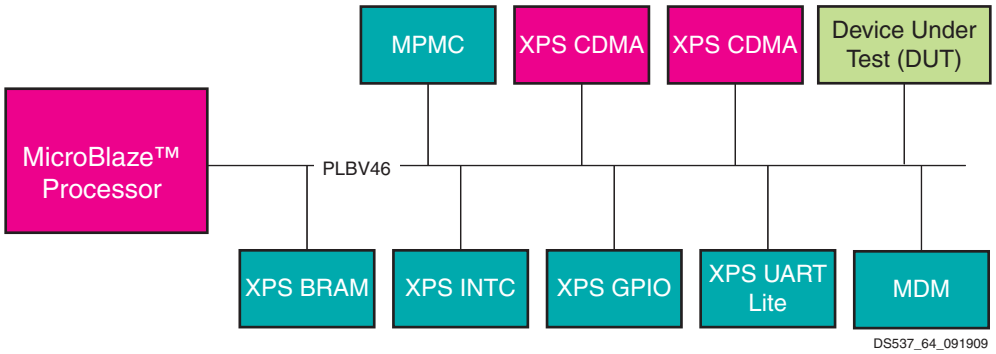

Figure 64: **Spartan-3A DSP FPGA System with the XPS LL TEMAC as the DUT**

The target FPGA was then filled with logic to drive the LUT and BRAM utilization to approximately 70% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target F_{MAX} numbers are shown in Table 143.

Table 143: **System Performance**

Target FPGA	Target F_{MAX} (MHz)
xc3sd3400a	90
xc6slx45t(1)	90
xc4vfx60	100
xc5vfx70t	120
xc6vlx240t	150

1. LUT utilization ~60%, BRAM utilization ~ 70%, I/O utilization ~80%

The target F_{MAX} is influenced by the exact system and is provided for guidance. It is not a guaranteed value across all systems.

Specification Exceptions

The XPS_LL_TEMAC design has no exceptions to the IEEE Std 802.3-2002 specification mandatory requirements.

Reference Documents

1. UG368 Virtex-6 Embedded Tri-Mode Ethernet MAC User Guide
2. UG194 Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide
3. UG074 Virtex-4 FPGA Embedded Tri-Mode Ethernet MAC User Guide v1.9
4. UG138 LogicCORE IP Tri-Mode Ethernet MAC User Guide v4.1
5. UG170 LogicCORE IP Ethernet Statistics User Guide
6. UG196 Virtex-5 FPGA RocketIO GTP Transceiver User Guide
7. UG366 Virtex-6 FPGA GTX Transceivers User Guide
8. DS568 XPS_LL_FIFO v1.02a
9. SP006 LocalLink Interface Specification
10. DS643 Multi-Port Memory Controller (MPMC) v5.04a
11. UG200 Embedded Processor Block in Virtex-5 FPGAs Reference Guide
12. UG625 Constraints Guide
13. UG492 LogicCORE IP Ethernet AVB Endpoint
14. Answer Record 32713
15. EDK Processor IP Reference Guide
16. IBM CoreConnect 128-Bit Processor Local Bus, Architectural Specification Version 4.6

Revision History

Date	Version	Revision
8/31/07	1.0	Initial Xilinx release.
9/28/07	1.1	Update for new revision and to add MII to soft TEMAC implementation as well as UCF constraint information and update clocking circuitry diagrams.
10/1/07	1.2	Added F_{MAX} Margin System Performance section.
10/3/07	1.3	Updated clocking circuitry diagrams, constraint information and implementation resource information.
10/12/07	1.4	Updated to core revision to 1.01a.
1/22/08	1.5	Final updates for release.
2/07/08	1.6	Updated core revision to 1.01b.
4/16/08	1.7	Added Automotive Spartan-3E, Automotive Spartan-3A, and Automotive Spartan-3A DSP support.
4/22/08	1.7	Final updates for release.
7/03/08	1.8	Updated RGMII clock diagrams and RGMII and GMII constraints to match design.
2/17/09	1.9	Updated with new functions for core version 2.00a.
3/03/09	1.10	Updated with new functions for core version 2.01a.
3/31/09	1.11	Updated for revision change to 2.01b.
6/24/09	1.12	Updated to v2.02a for EDK_L 11.2 release: updated legal matter and copyright information, moved constraint examples to AR#32713, removed C_INCLUDE_IO diagrams and reference User Guides, updated supported devices.
7/17/09	2.0	Added Ethernet AVB to features, updated resource usage, added Hard TEMAC dependency with C_INCLUDE_IO parameter, updated Margin System figures.
12/2/09	2.1	Updated core revision to 2.03a for EDK_L 11.4 release; updated images; converted to current data sheet template. Incorporated CR523738 by adding clarification that half-duplex is not supported.
12/10/09	2.2	Incorporated CR523738 to add clarification that half-duplex is not supported.
4/01/10	2.3	Update V6 and S6 resource utilization tables Table 138 and Table 141 to indicate 6-Input LUTs.
5/17/10	2.4	Incorporated CR560051 (C_INCLUDE_IO with Soft TEMAC)
6/23/10/10	2.5	Incorporated CR480350 to update SOP and EOP terminology.

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